

MODEL NAME : *VAR00*  
PCB NO : *LA-9201P*  
BOM P/N : *4619K031L01*  
*4619K031L02*

# Dell/Compal Confidential

Mariner 14

## Schematic Document

DISCRETE VGA N14P-GT and N14E-GE (optimus)

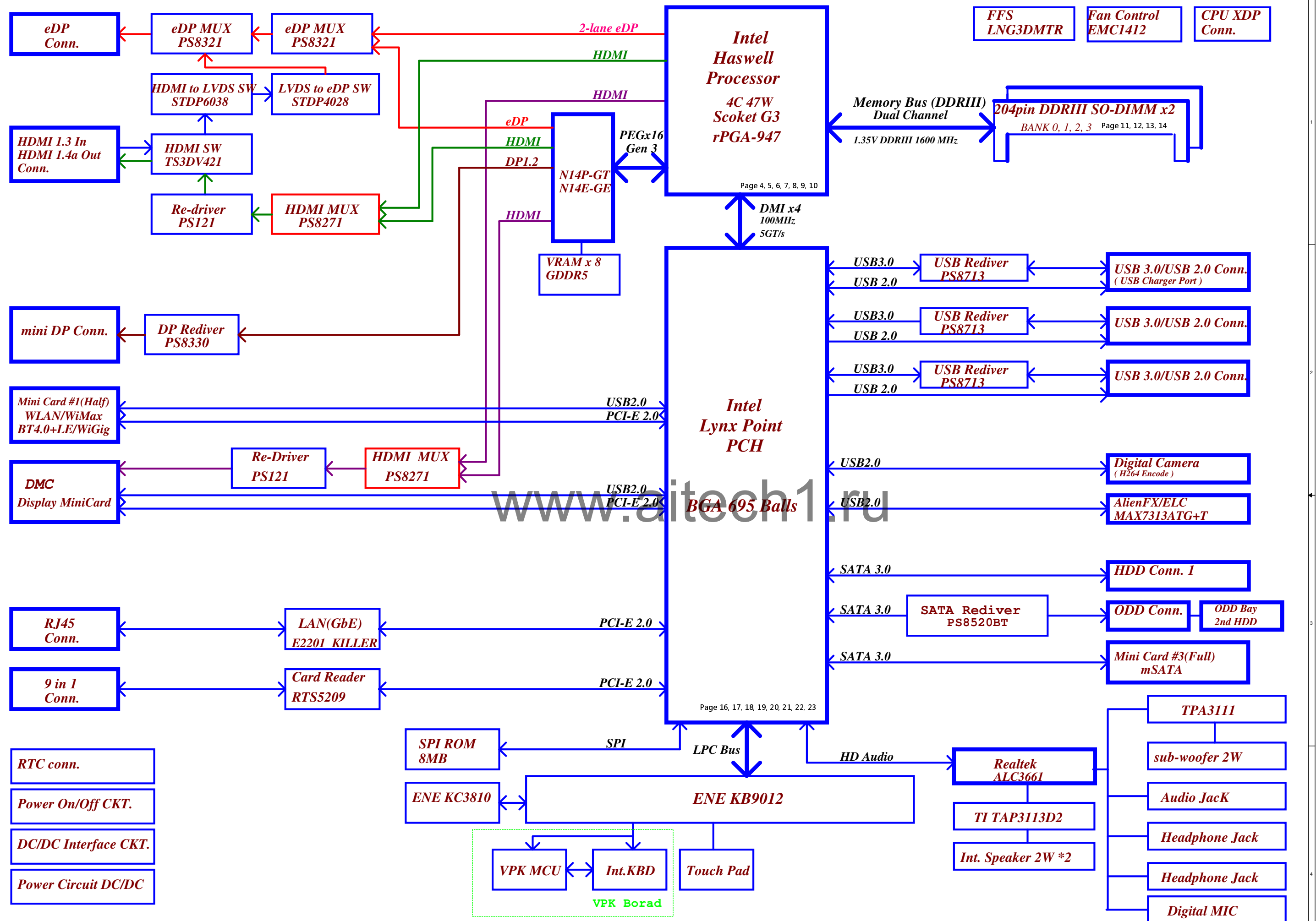
2012-06-06

Rev: 0.1

Highlight the short pad for 0 ohm

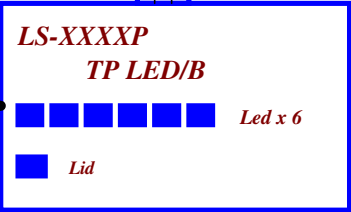
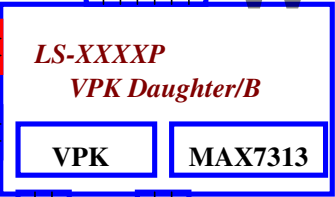
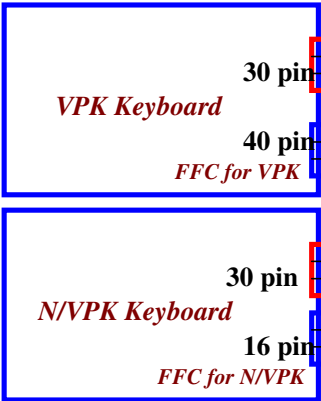
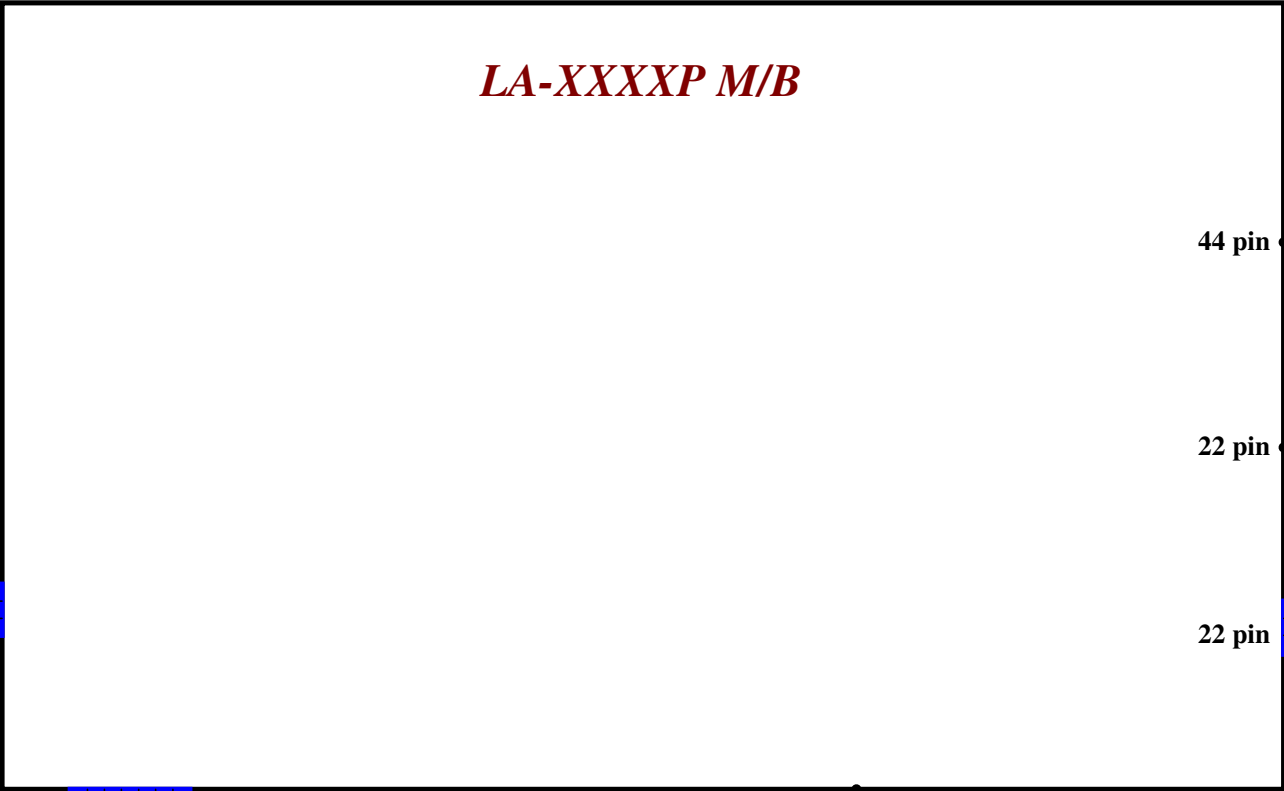
CONN@ Connector Component  
up@ Upsell  
en@ Entry  
X76@ VARM(SAMSUNG, Hynix)  
N14P@ N14P-GT  
N14E@ N14E-GE

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Project Code : VAR00  
File Name : LA-9201P



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Board ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra	100K +/- 5%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

BOARD ID Table

Board ID	PCB Revision
0	0.1 (SSI)
1	0.2 (PT)
2	0.3 (ST)
3	0.4 (QT)
4	1.0 (MP)
5	
6	
7	

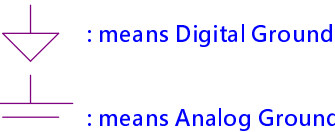
POWER STATES

Signal	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
State									
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM) / M-OFF	LOW	HIGH		HIGH	LOW	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

PM TABLE

power plane	+5VALW +3VALW +3VLP +3V_PCH	+1.5V	+5VS +3VS +1.8VS +1.5VS +0.75VS +3VMXM +5VMXM +VCCP +VCCSA +VCC_CORE +1.5V_CPU_VDDQ
State			
S0	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

Symbol Note :



USB2.0

USB PORT#	DESTINATION
0	JUSB1(USB3.0 P1)
1	JUSB2(USB3.0 P2)
2	JUSB3(USB3.0 P3)
3	JUSB4(USB3.0 P4)
4	JMINI1 (WLAN)
5	JMINI2 (DMC)
6	AlienFX/ELC
7	IR SENSOR
8	Bluetooth
9	JESATA
10	None
11	eDP CAMERA
12	LVDS CAMERA
13	VPK K/B

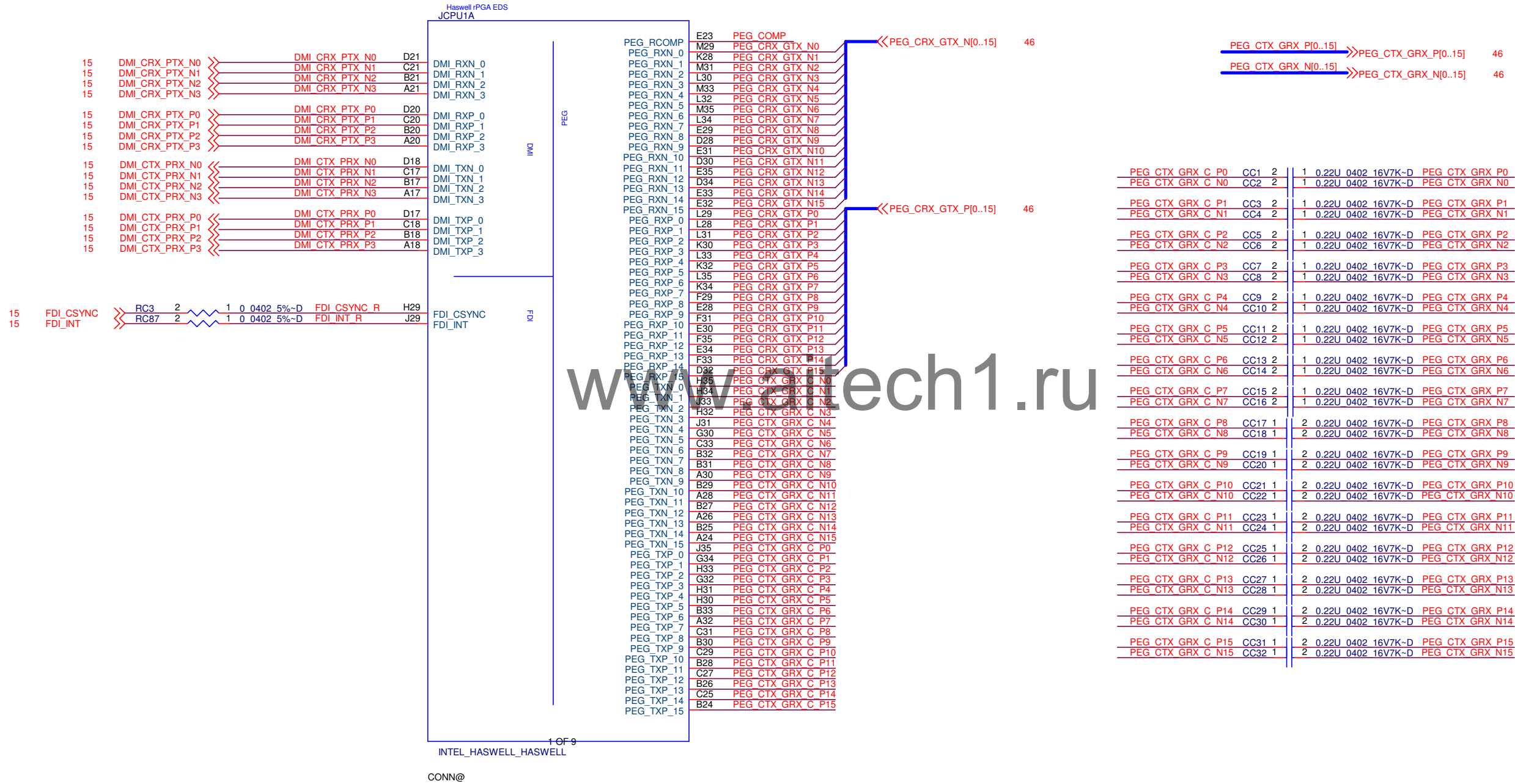
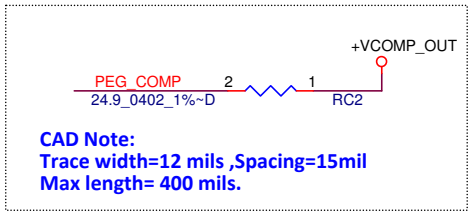
DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
CLKOUT_PCIE0	MINI CARD-1 WLAN	CLKOUTFLEX0	None
CLKOUT_PCIE1	MINI CARD-2 DMC	CLKOUTFLEX1	None
CLKOUT_PCIE2	10/100/1G LAN	CLKOUTFLEX2	None
CLKOUT_PCIE3	CARD READER	CLKOUTFLEX3	None
CLKOUT_PCIE4	None		
CLKOUT_PCIE5	None		
CLKOUT_PCIE6	None		
CLKOUT_PCIE7	None		
CLKOUT_PEG_A	NV		

CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC
PCI2	80port debug card
PCI3	None
PCI4	None

SATA III	DESTINATION
SATA0	HDD1
SATA1	None
SATA2	ODD
SATA3	mSATA
SATA4	MINI CARD-1 WLAN
SATA5	MINI CARD-2 MDC

PCI EXPRESS	DESTINATION
Lane 1	None
Lane 2	None
Lane 3	10/100/1G LAN
Lane 4	CARD READER
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None

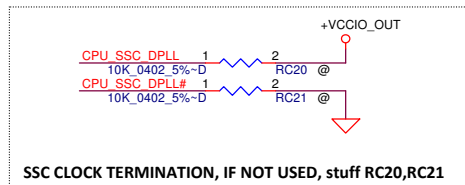
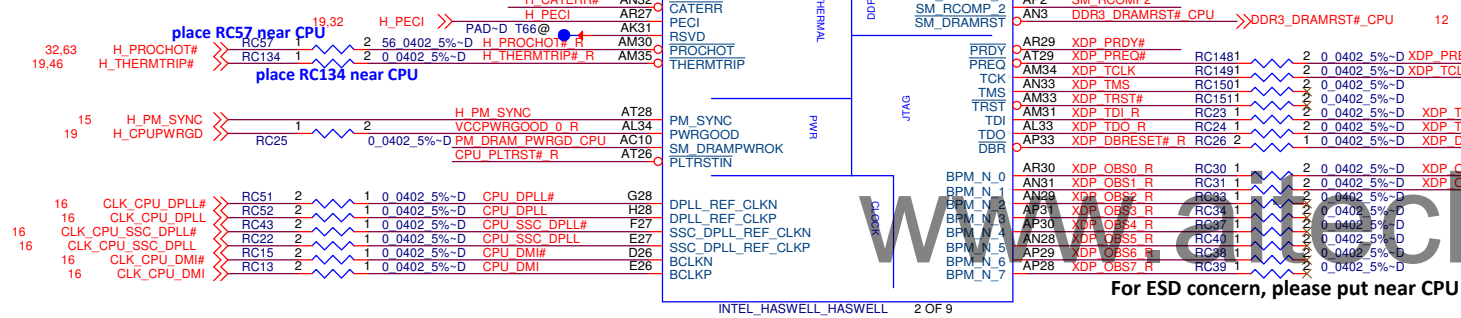
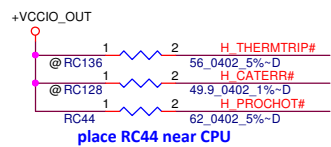
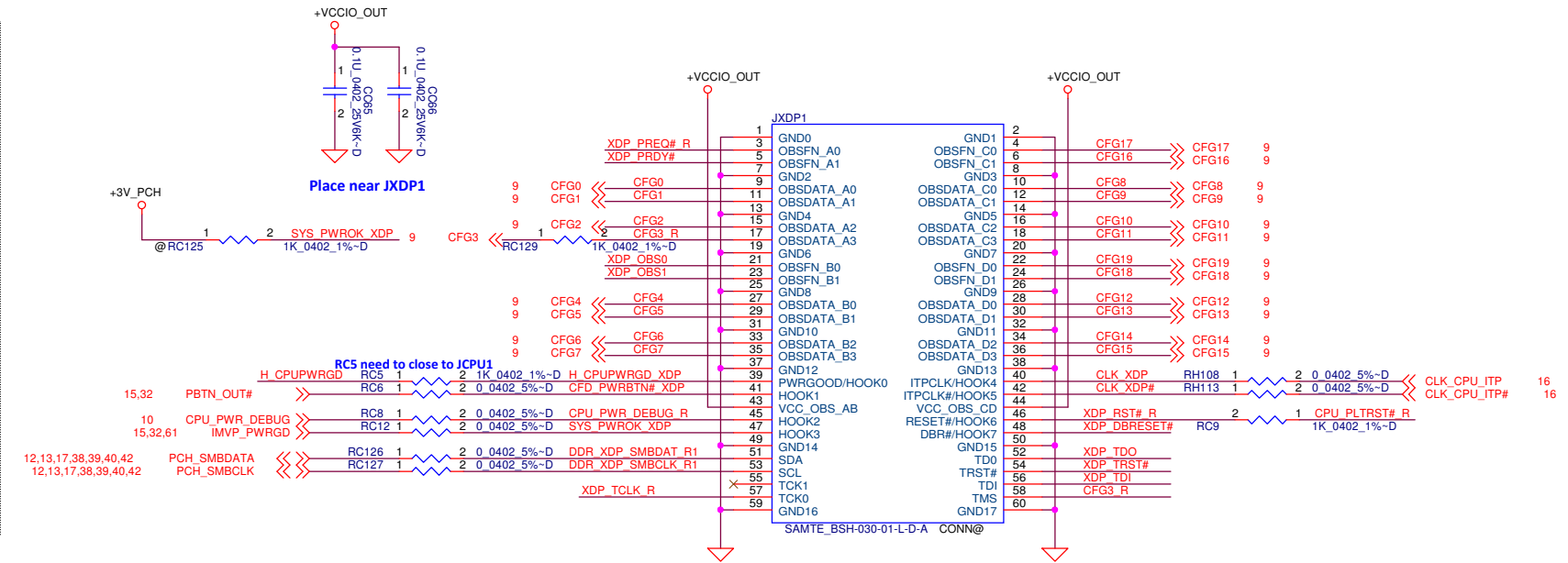




### 15 SM\_DRAMPWROK with DDR Power Gating Topology

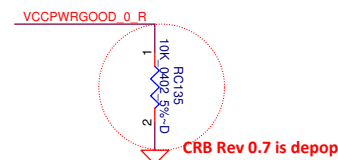
The diagram illustrates the SM\_DRAMPWROK with DDR Power Gating Topology. Key components and connections include:

- UC2 (74AHC1G09GW\_TSSOP-5):** A 1-input CMOS inverter used for signal inversion.
- Power Supplies:**
  - +3V\_PCH:** Provides power to RC89, RC18, and RC36.
  - +3V\_PCH:** Provides power to the inverter UC2.
  - +1.35V\_CPU\_VDDQ:** Provides power to RC16, RC28, and RC14.
  - 10.45V:** Provides power to the CPU (OC1).
- Resistors:**
  - RC89 (100k):** Connected to +3V\_PCH and the inverter input.
  - RC88:** Connected to SYS\_PWROK and the inverter input.
  - RC18 (200):** Connected to +3V\_PCH and the inverter input.
  - RC36:** Connected to the inverter output and the CPU (OC1).
  - RC16 (1.8k):** Connected to +1.35V\_CPU\_VDDQ and the CPU (OC1).
  - RC28 (3.3k):** Connected to +1.35V\_CPU\_VDDQ and the CPU (OC1).
  - RC14 (3.3k):** Connected to +1.35V\_CPU\_VDDQ and the CPU (OC1).
  - RC64 (39):** Connected to the CPU (OC1).
- Capacitors:**
  - CC156 (0.1uF):** Connected to +3V\_PCH.
- Signals:**
  - SYS\_PWROK:** Input signal to the inverter.
  - PM\_DRAM\_PWRGD:** Input signal to the inverter.
  - RUNPWROK AND:** Output signal from the inverter.
  - RUN\_ON\_CPU1.5VS3#:** Input signal to the CPU (OC1).



### Buffered reset to CPU

**CAD Note:**  
PLACE PULL-UP RESISTOR WITHIN 2 INCH OF THE CPU

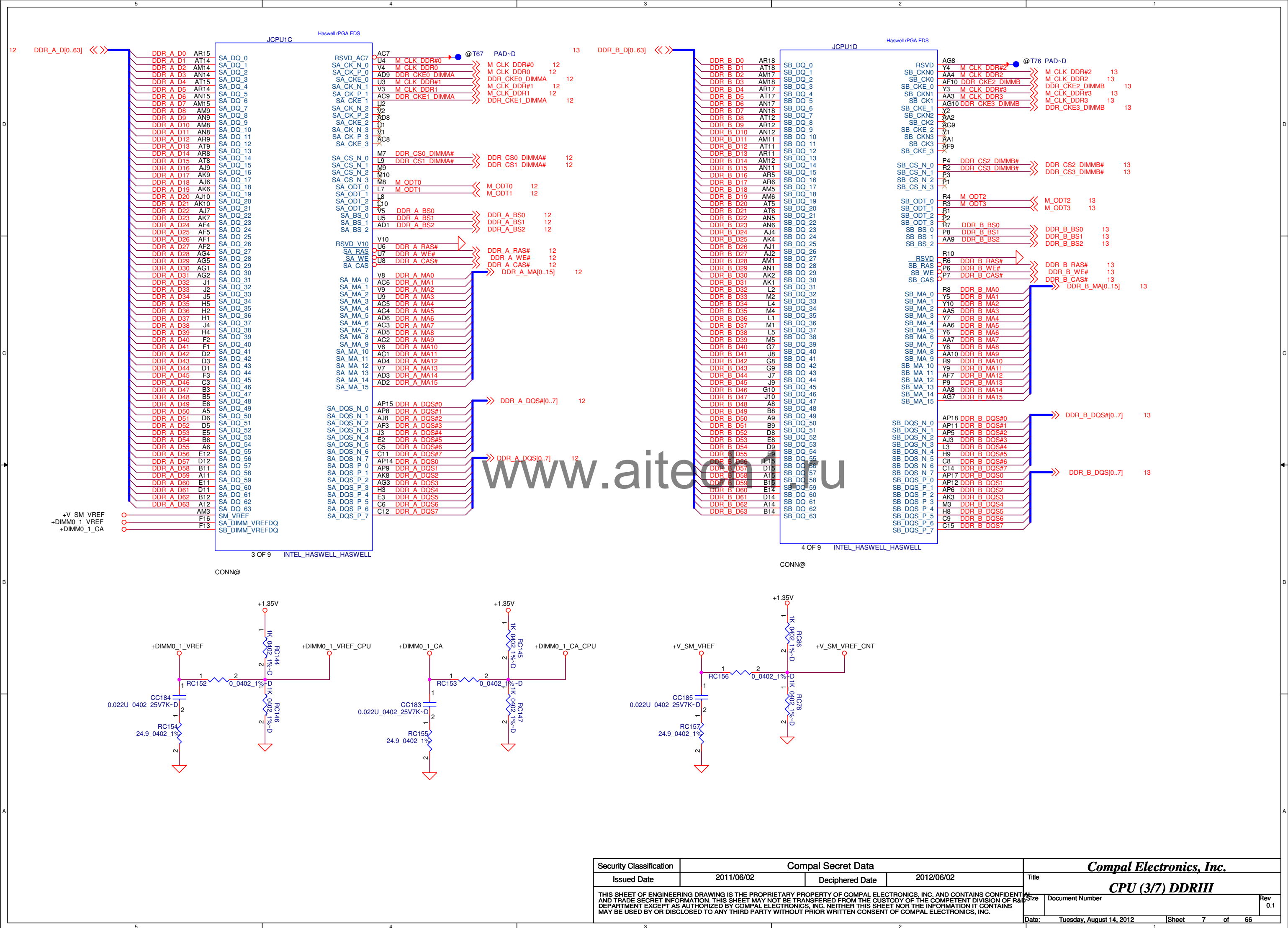


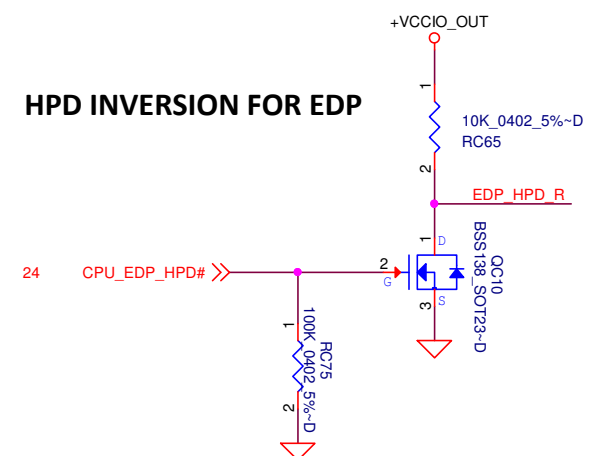
**CAD Note:**  
Avoid stub in the PWRGD path  
while placing resistors RC25 & RC130

**CAD Note:**  
Trace width=12~15 mil, Spacing=20 mils  
Max trace length= 500 mil

Timing diagram for the RC19-RC41 pins of the XDP module. The diagram shows signals XDP\_DBRESET#, XDP\_TMS, XDP\_TDI R, XDP\_PREQ#, XDP\_TDO R, XDP\_TCLK, and XDP\_TRST# over time. The signals are connected to pins RC19, RC27, RC29, RC32, RC35, RC42, and RC41 respectively. The diagram includes voltage levels of +3VS and +1.05VS, and a ground symbol. A red oval highlights the XDP\_TDI R signal.

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				Part Number Document Number LA-9201P	Rev 0.1	
3		2		Date: Tuesday, August 14, 2012	Sheet 8 of 66	1



CFG6

CFG5

1

2


1 @RC90 2

1K\_0402\_1%-D

CFG7

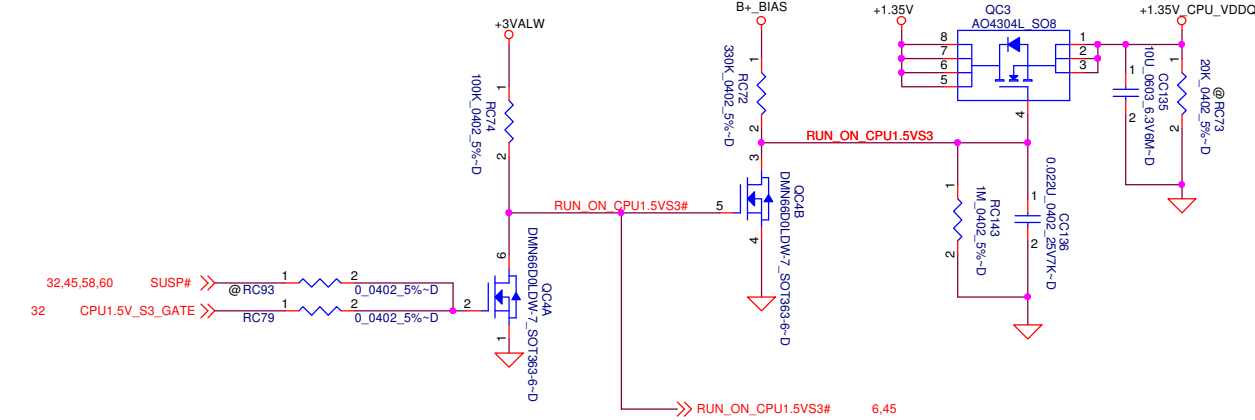
1k 0.002 1%~D @RC91

1 2

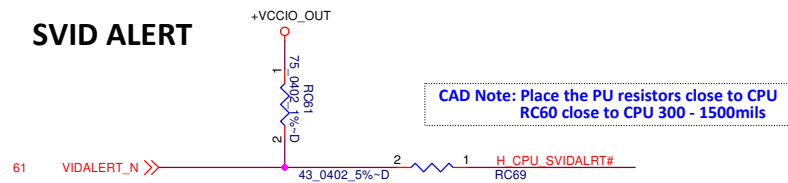




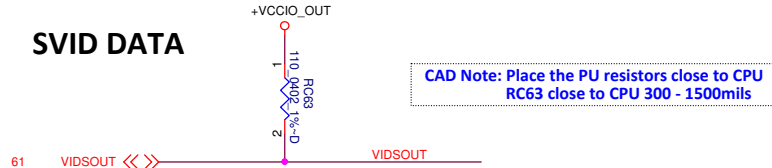
## +1.35V\_CPU\_VDDQ Source



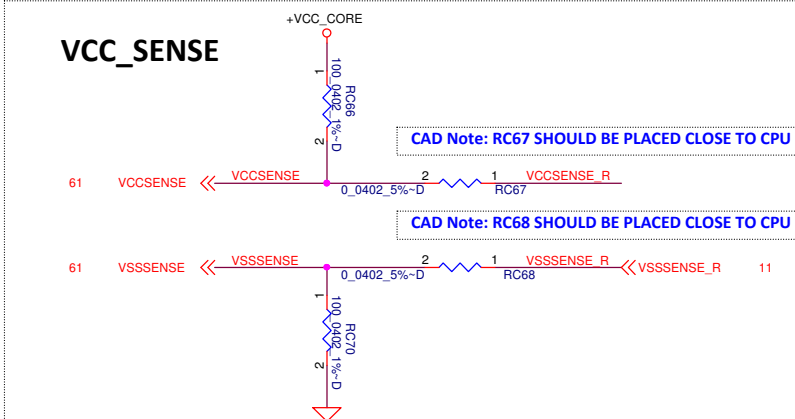
## SVID ALERT



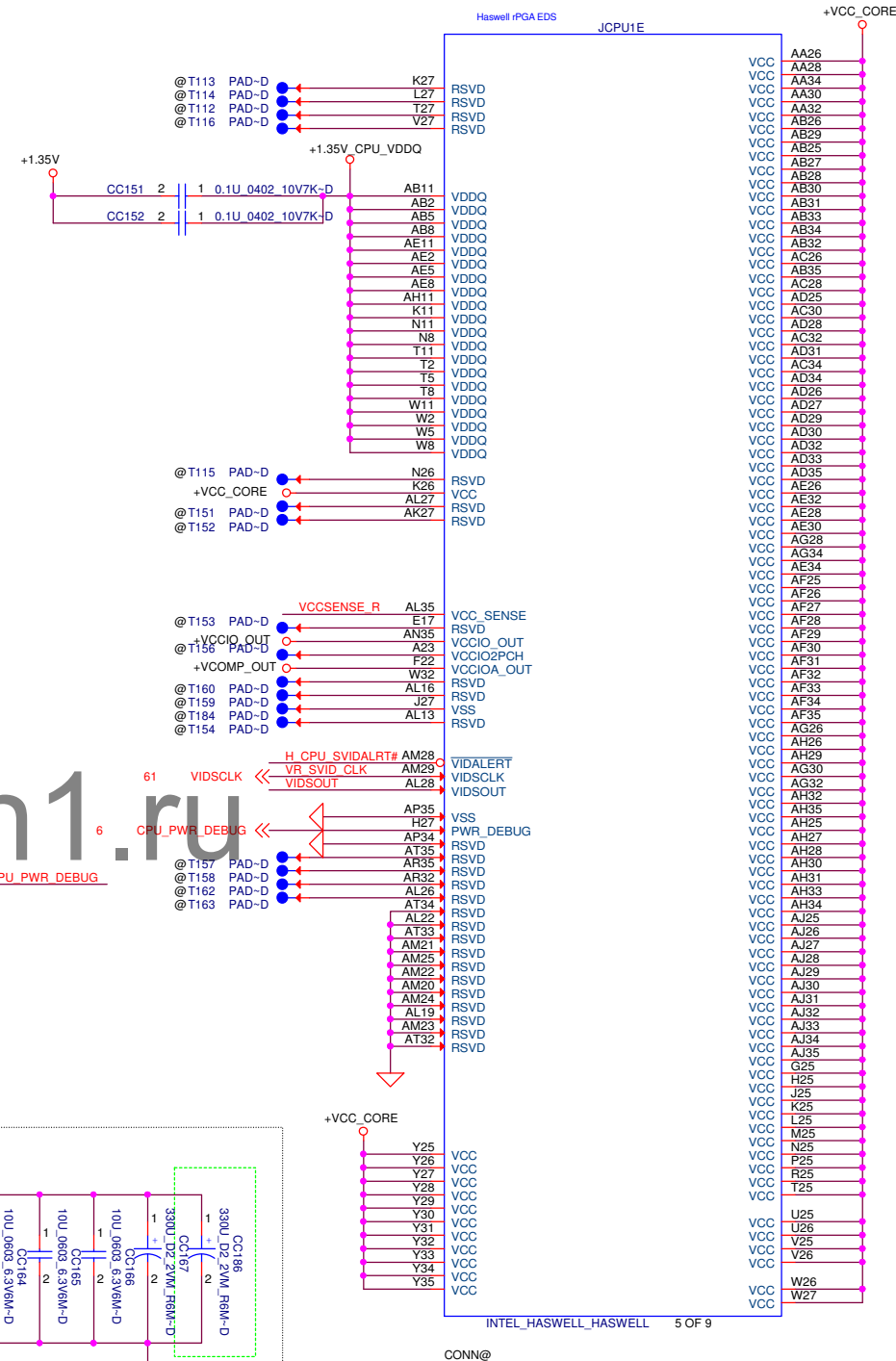
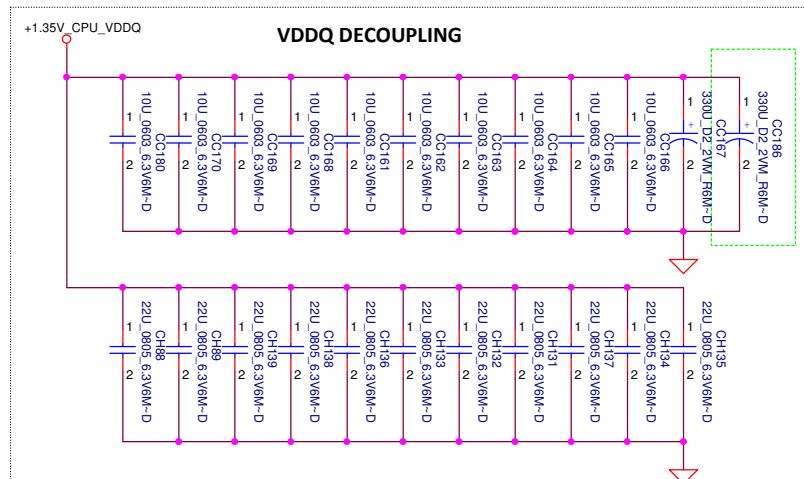
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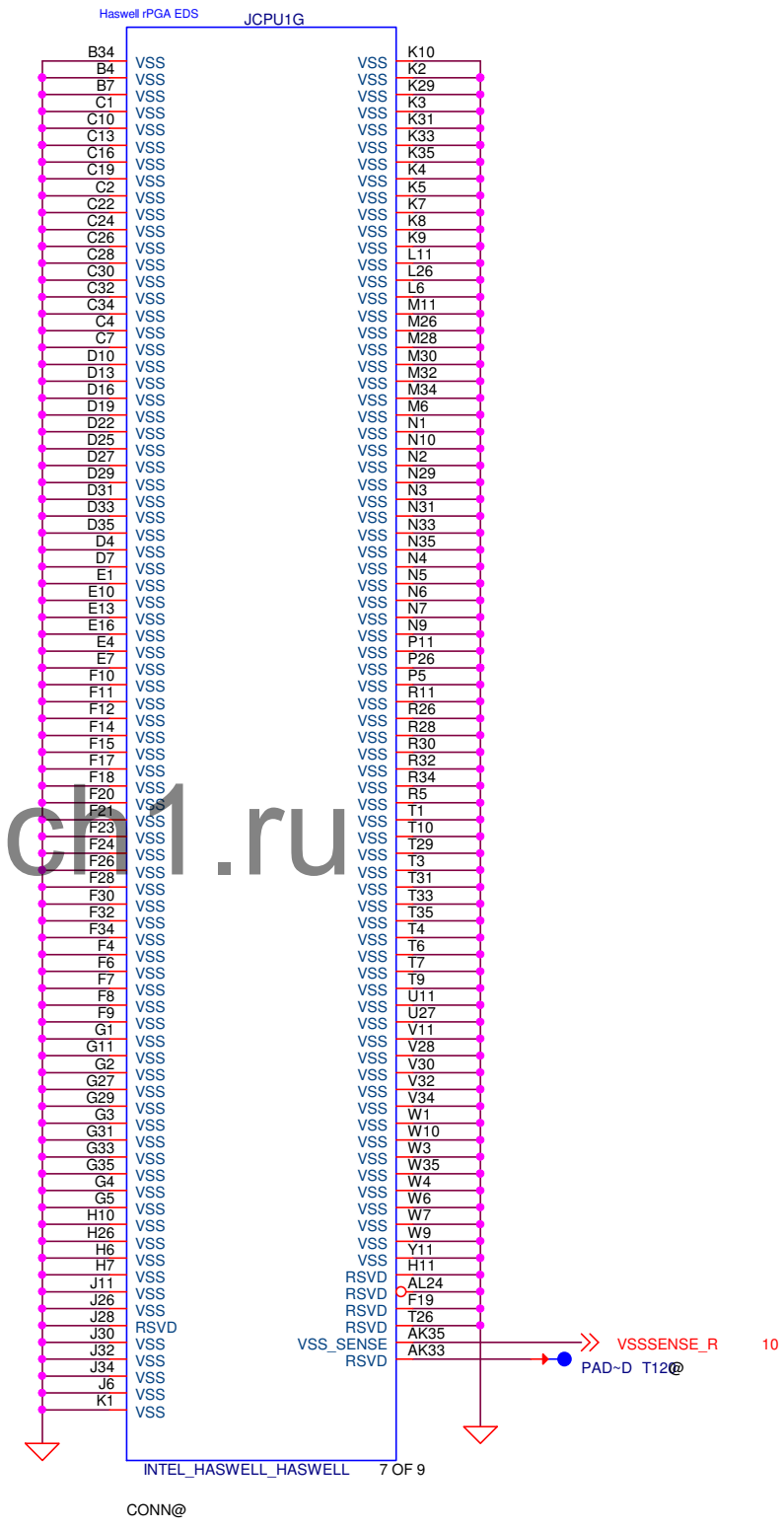
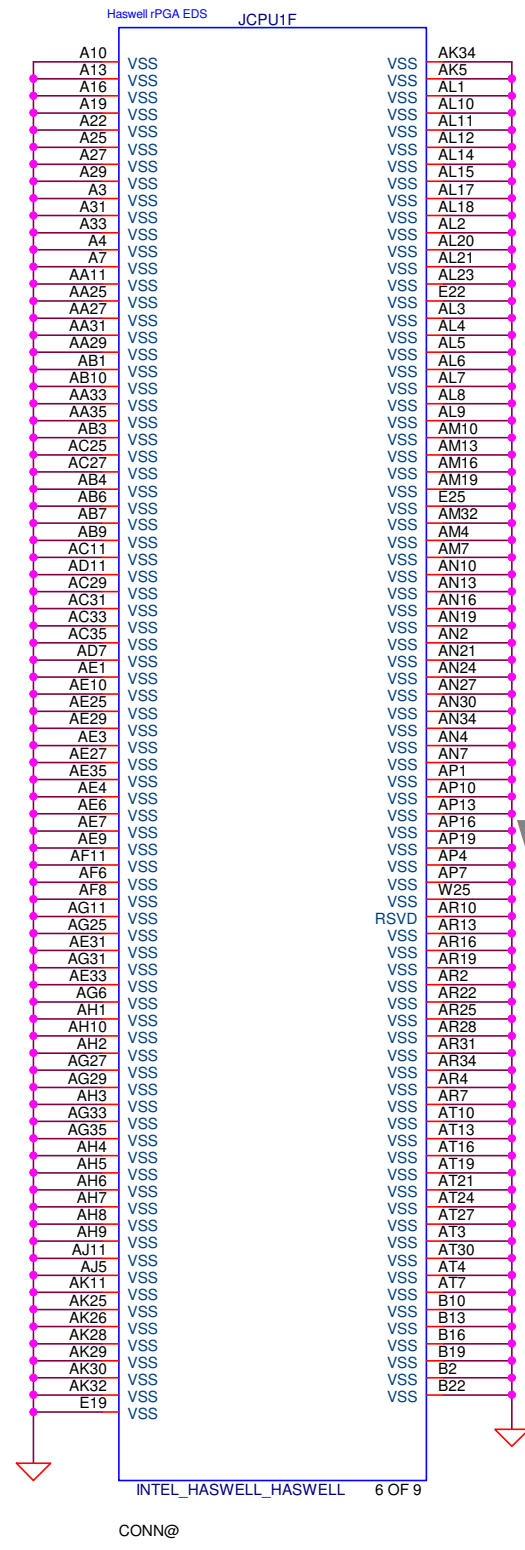


## VCC\_SENSE



## VDDQ DECOUPLING

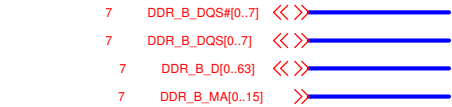








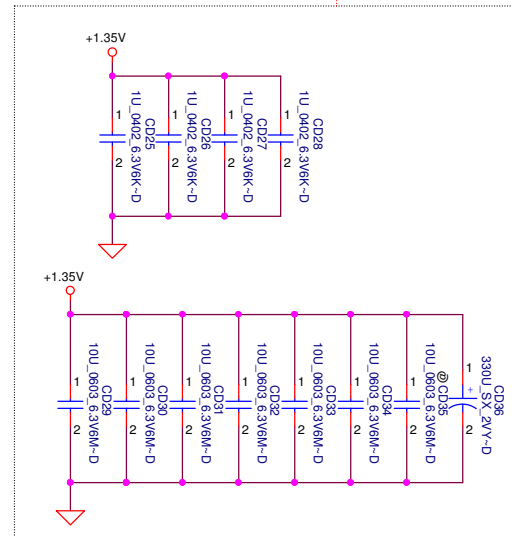
2011/11/25 change to +1.35V



Note:  
Check voltage tolerance of  
VREF\_DQ at the DIMM socket

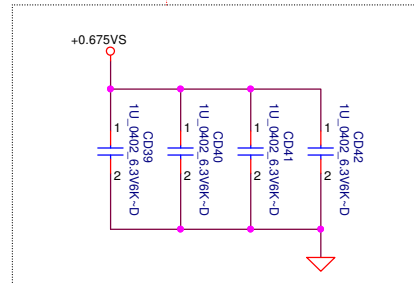
Layout Note:  
Place near JDIMMB

2011/11/25 change to +1.35V

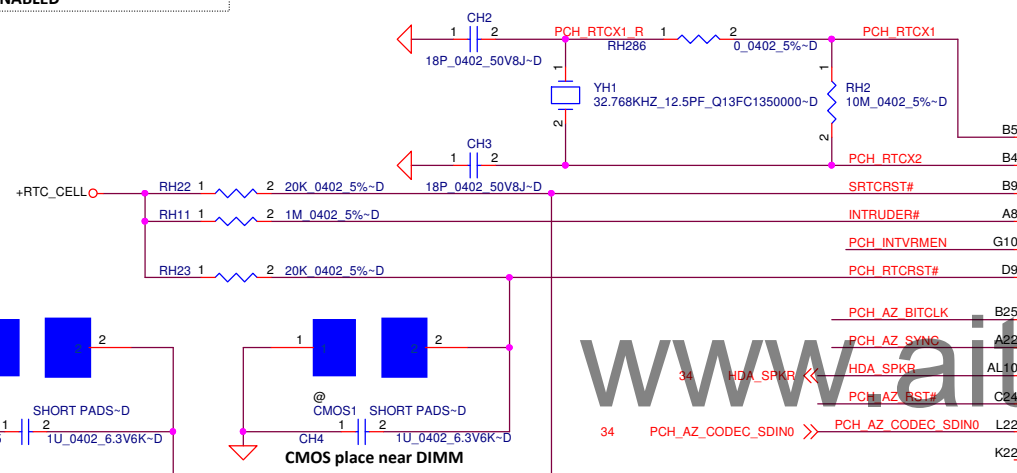
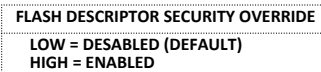
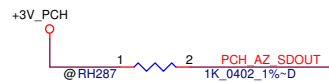
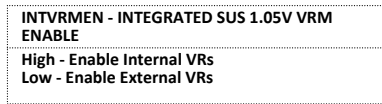


Layout Note:  
Place near JDIMMB.203,204

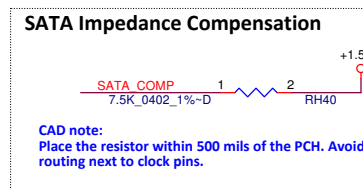
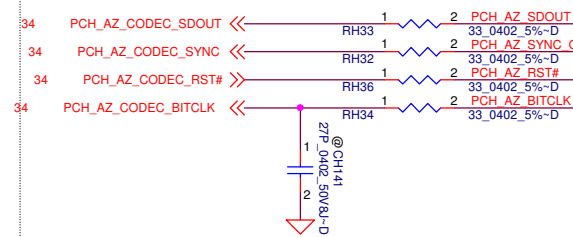
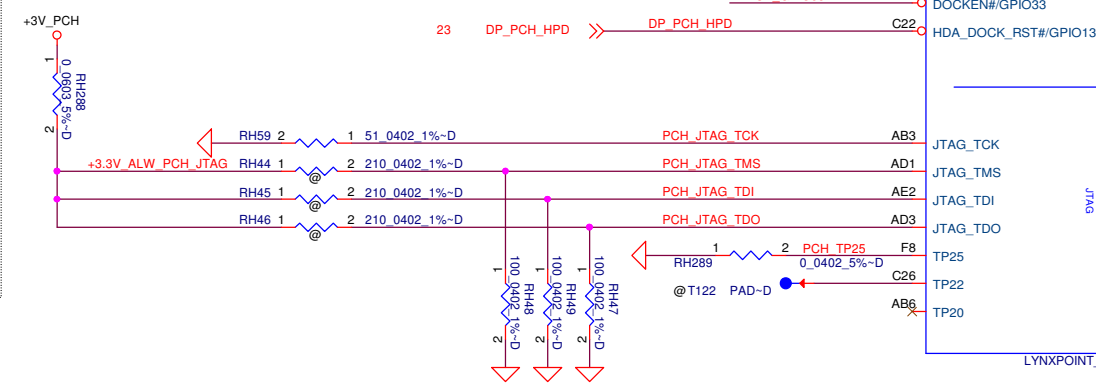
2011/11/25 change to +0.675V



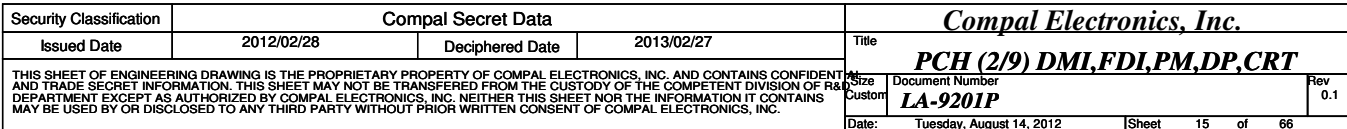
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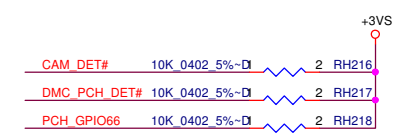
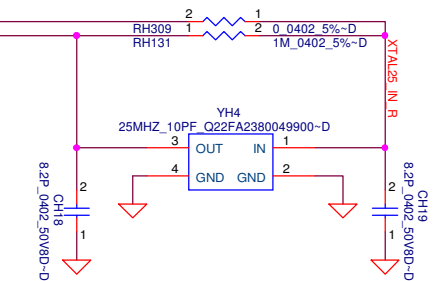
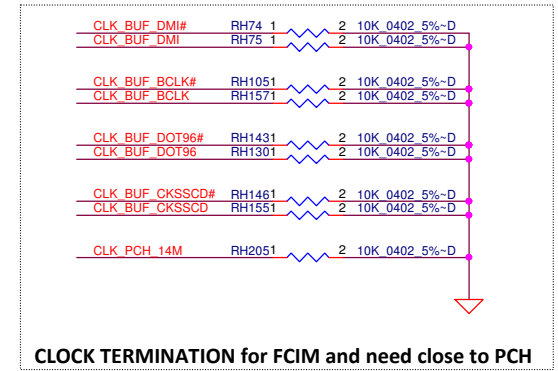
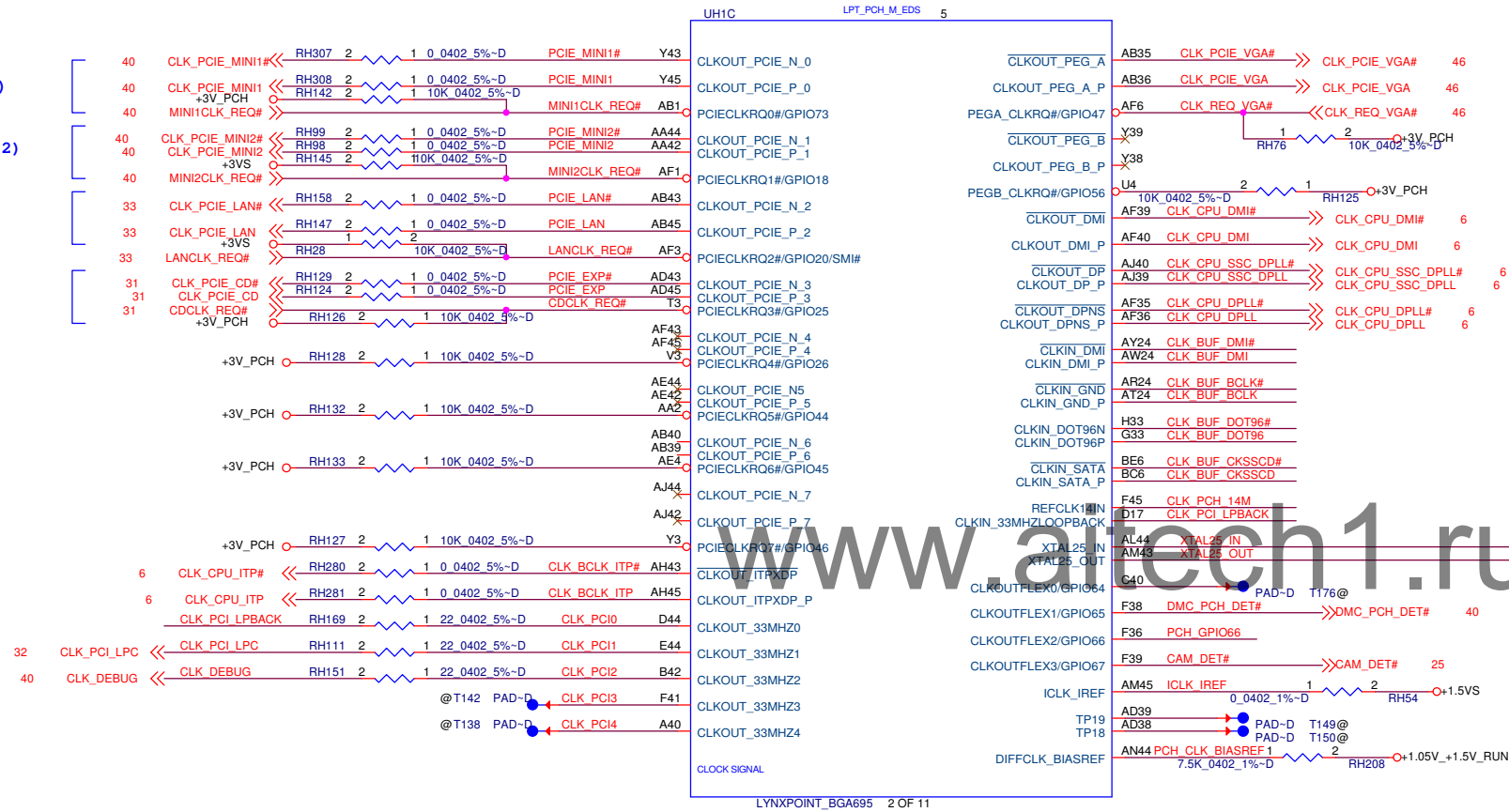
ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers



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MiniWLAN  
(Mini Card 1)  
  
DMC (Mini Card 2)  
  
10/100/1G LAN  
  
Card Reader

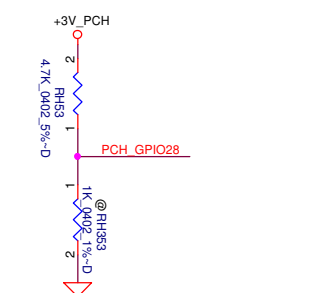
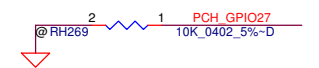
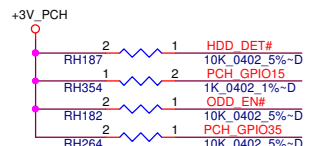
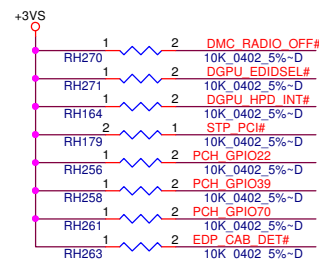




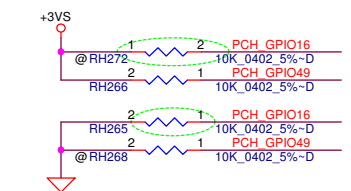




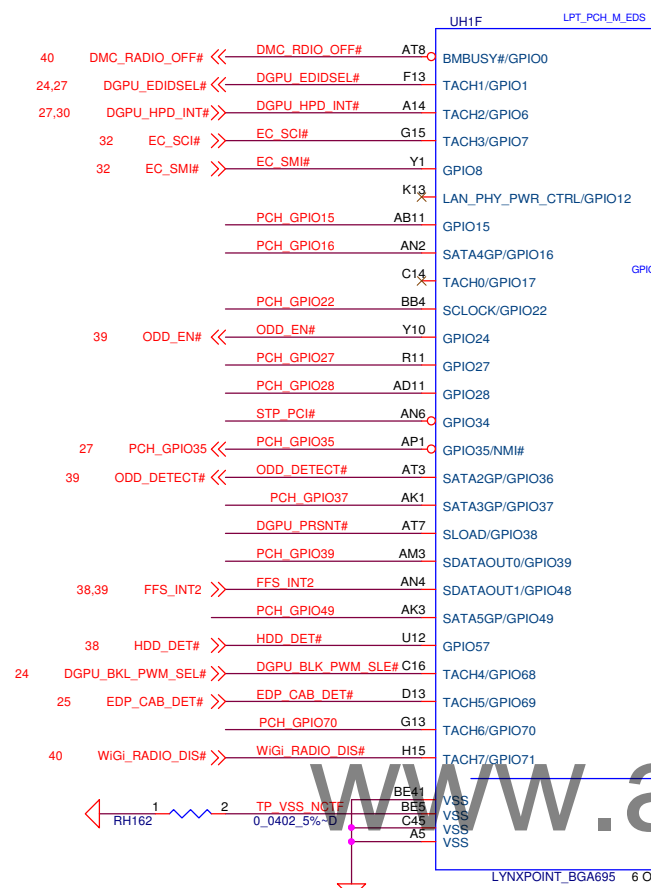




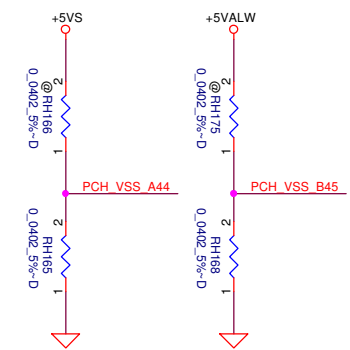
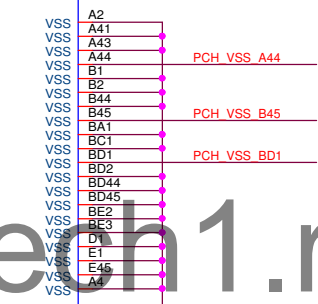
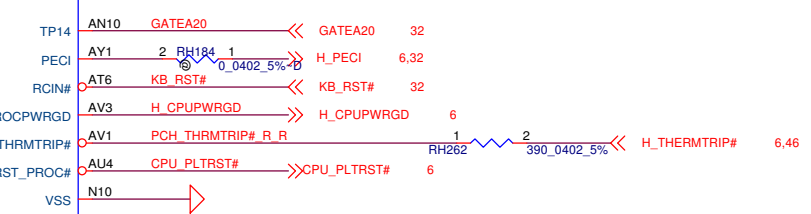
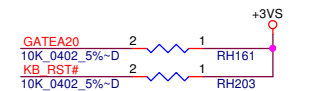
PLL ON DIE VR ENABLE  
ENABLED - HIGH(DEFAULT)  
DISABLED - LOW



Config	GPIO16,49
USB X4,PCIEX8,SATAx6	11
USB X6,PCIEX8,SATAx4	01

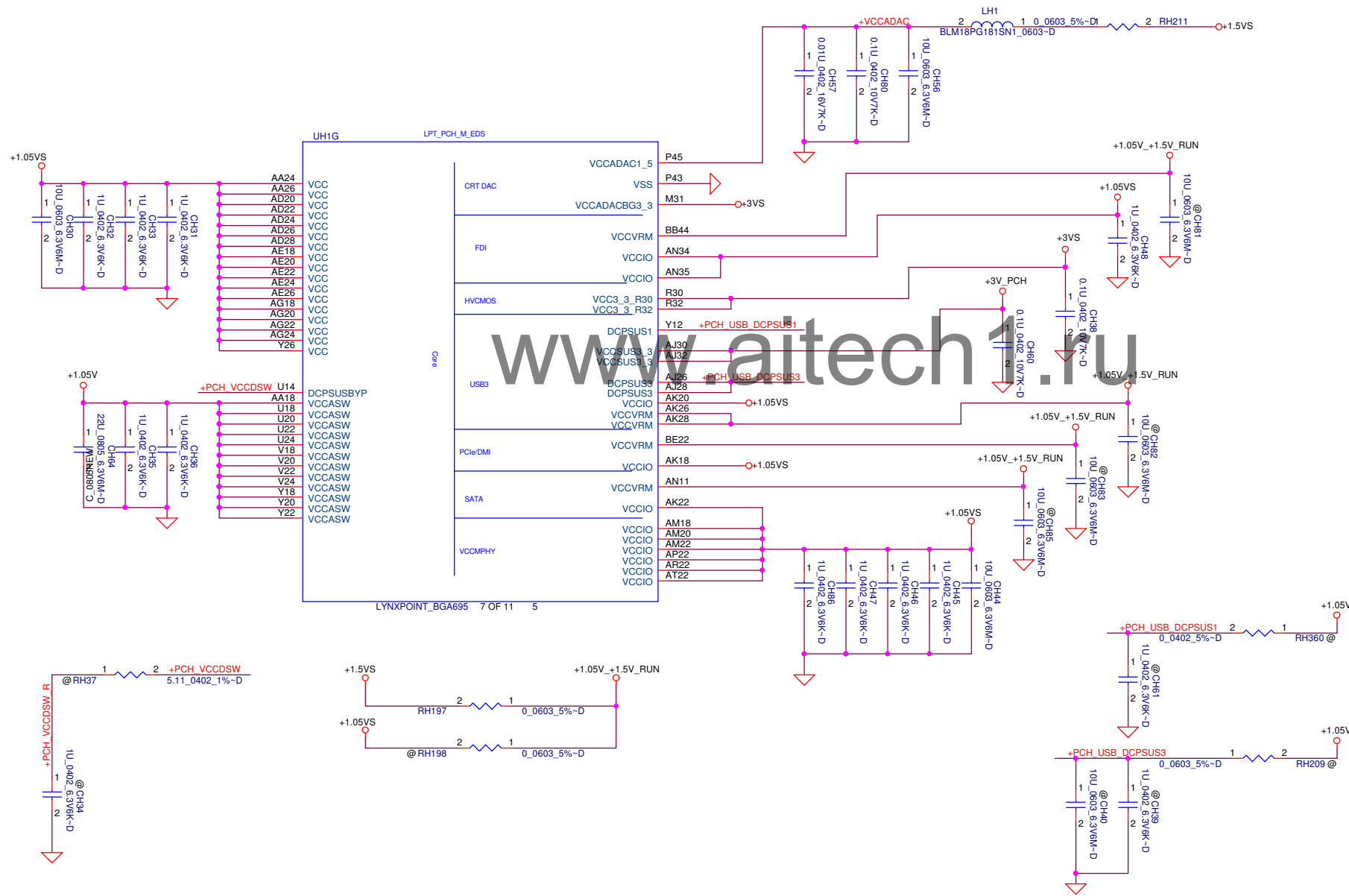


For BIOS setting dGPU present  
\* LOW - dGPU exist

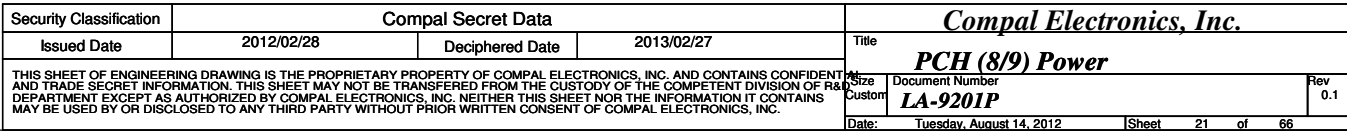


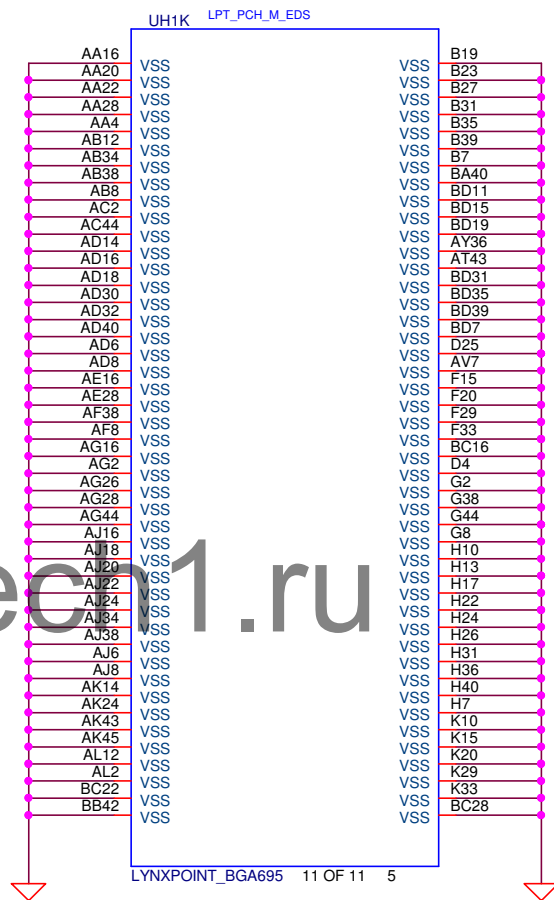
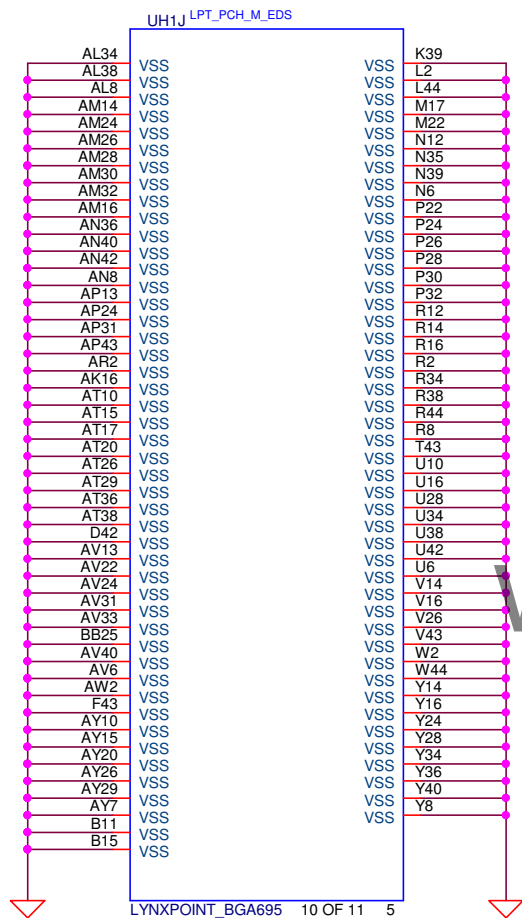
SATA2GP/GPIO36, SATA3GP/GPIO37 SAMPLED AT RISING EDGE OF PWROK.  
WEAK INTERNAL PULL-DOWN.(WEAK INTERNAL PULL-DOWN IS DISABLED AFTER PLRST\_N DE-ASSERTS).  
NOTE: THIS SIGNAL SHOULD NOT BE PULLED HIGH WHEN STRAP IS SAMPLED.

Fixed Signals				Muxed Signals		Fixed Signals						Muxed Signals		Fixed Signals			
USB3 1	USB3 2	USB3 5	USB3 6	PCIE 1	PCIE 2	PCIE 3	PCIE 4	PCIE 5	PCIE 6	PCIE 7	PCIE 8	SATA 4	SATA 5	SATA 0	SATA 1	SATA 2	SATA 3
				(00)	(00)							(00)	(00)				
				USB3 3	USB3 4							PCIE 1	PCIE 2				
				(01)	(01)							(01)	(01)				

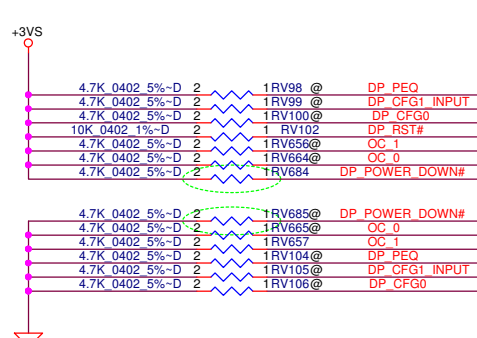
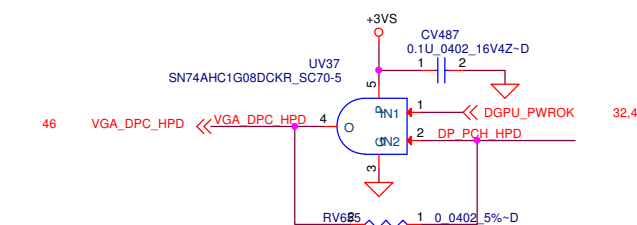


PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCADAC1_5	1.5V	0.070 A
VCCADAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK3_3	3.3V	0.055 A
VCCVRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A



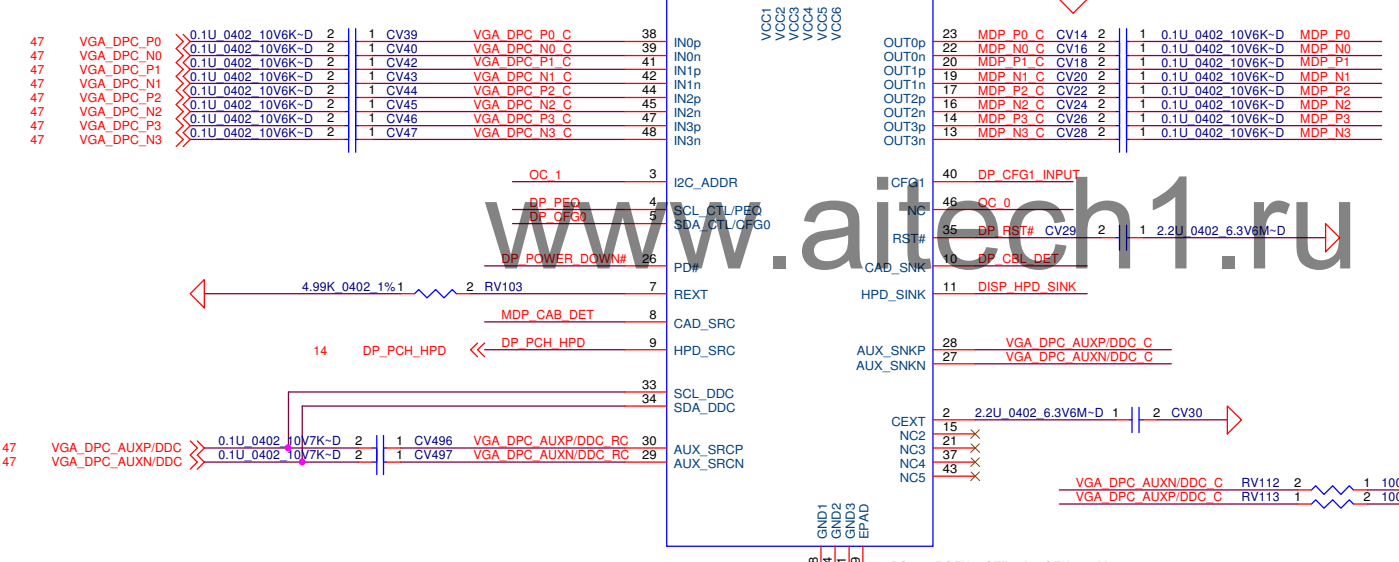


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				LA-9201P	0.1
				Date: Tuesday, August 14, 2012	Sheet 22 of 66

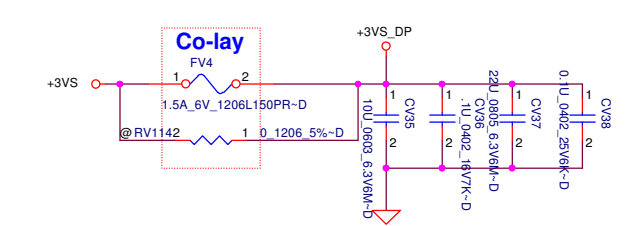


## DP Redriver

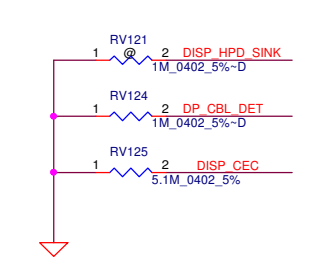
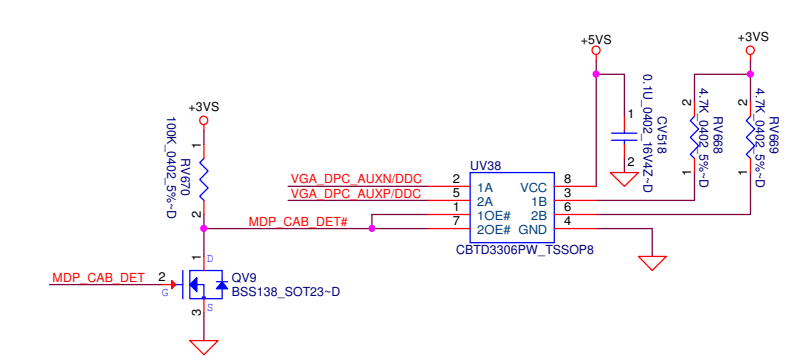
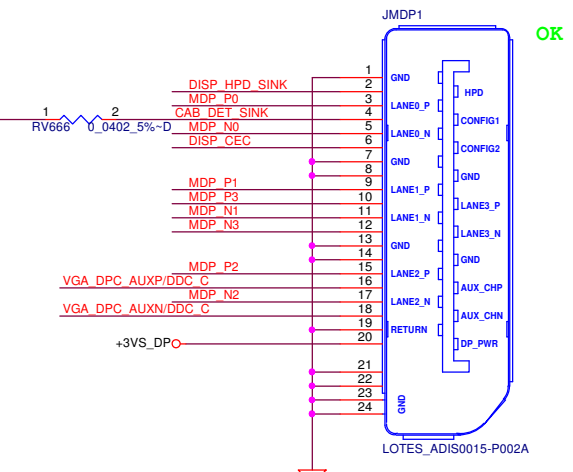
GPU

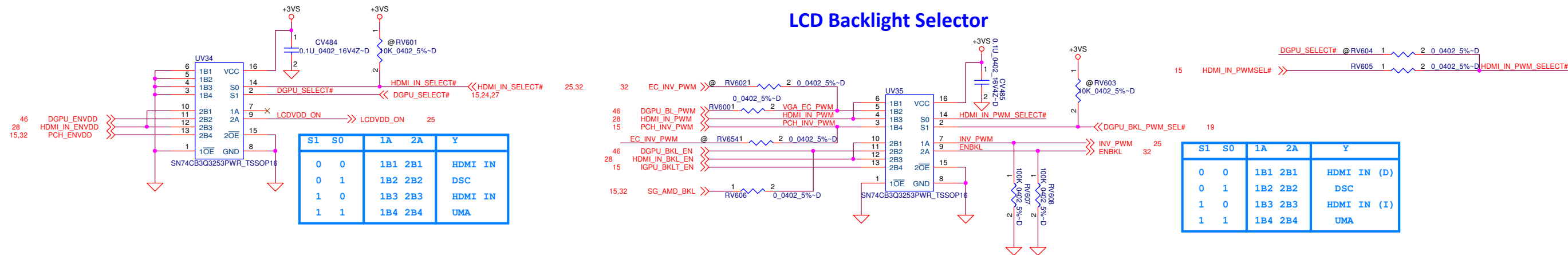


Need apply CIS part

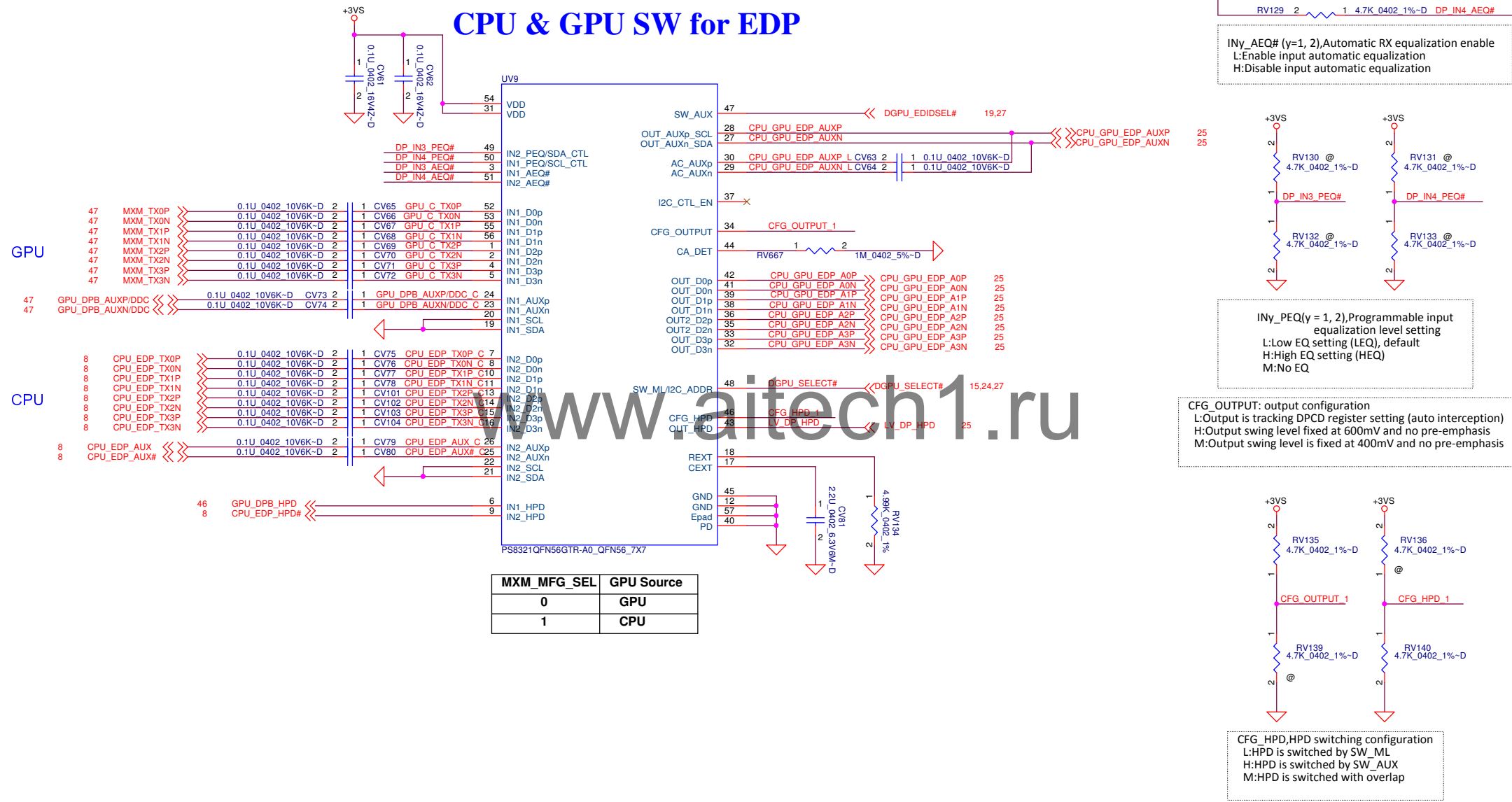


## Mini DP CONN





## CPU & GPU SW for EDP



INy\_AEQ# (y=1, 2), Automatic RX equalization enable  
L: Enable input automatic equalization  
H: Disable input automatic equalization

INy\_PEQ# (y=1, 2), Programmable input equalization level setting  
L: Low EQ setting (LEQ), default  
H: High EQ setting (HEQ)  
M: No EQ

CFG\_OUTPUT: output configuration  
L: Output is tracking DPCD register setting (auto interception)  
H: Output swing level fixed at 600mV and no pre-emphasis  
M: Output swing level is fixed at 400mV and no pre-emphasis

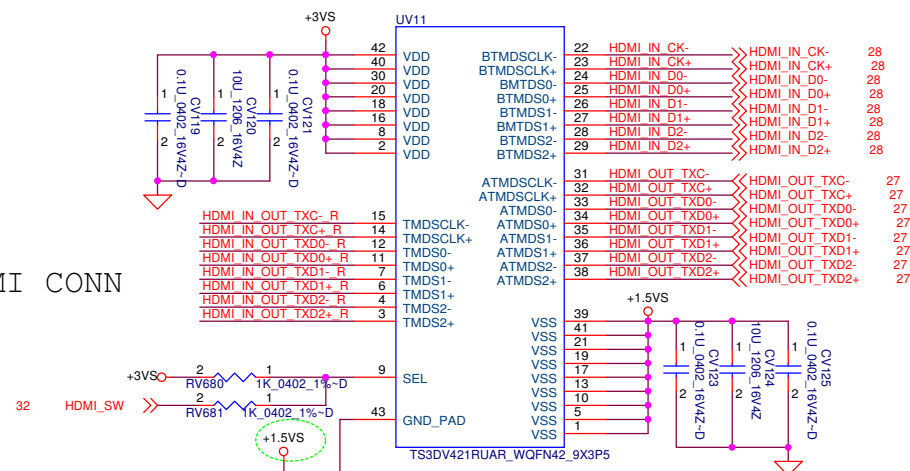
CFG\_HPD: HPD switching configuration  
L: HPD is switched by SW\_ML  
H: HPD is switched by SW\_AUX  
M: HPD is switched with overlap



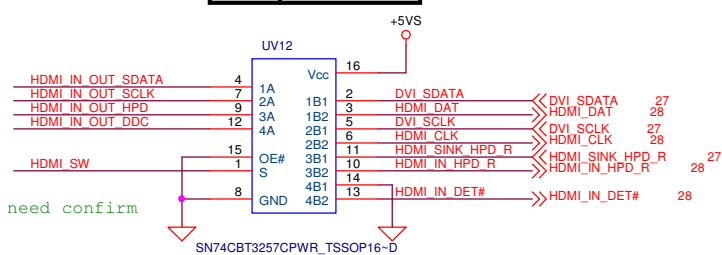




## HDMI CONN



SEL	OUTPUT
L	A
H	B

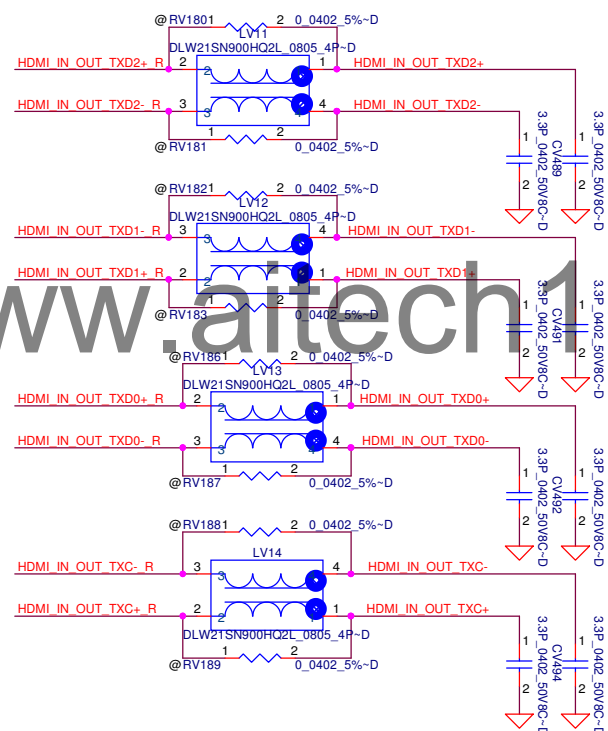
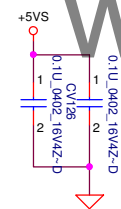


SEL	OUTPUT
L	B1
H	B2

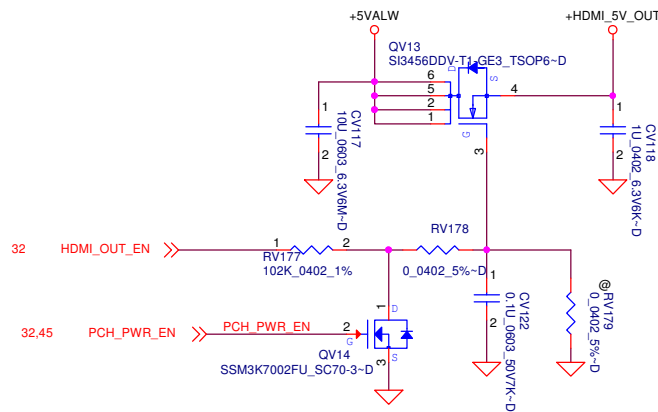
2011/11/30 need confirm  
with PCH

STDP6038

CPU/GPU



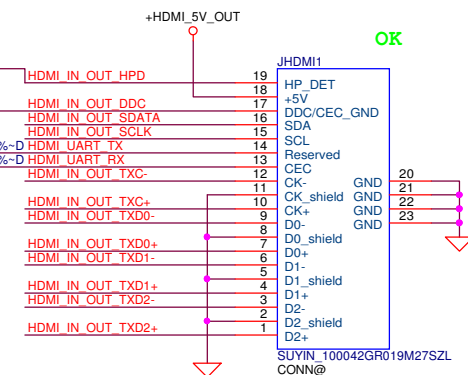
Reserve for EMI please close to JHDMI1



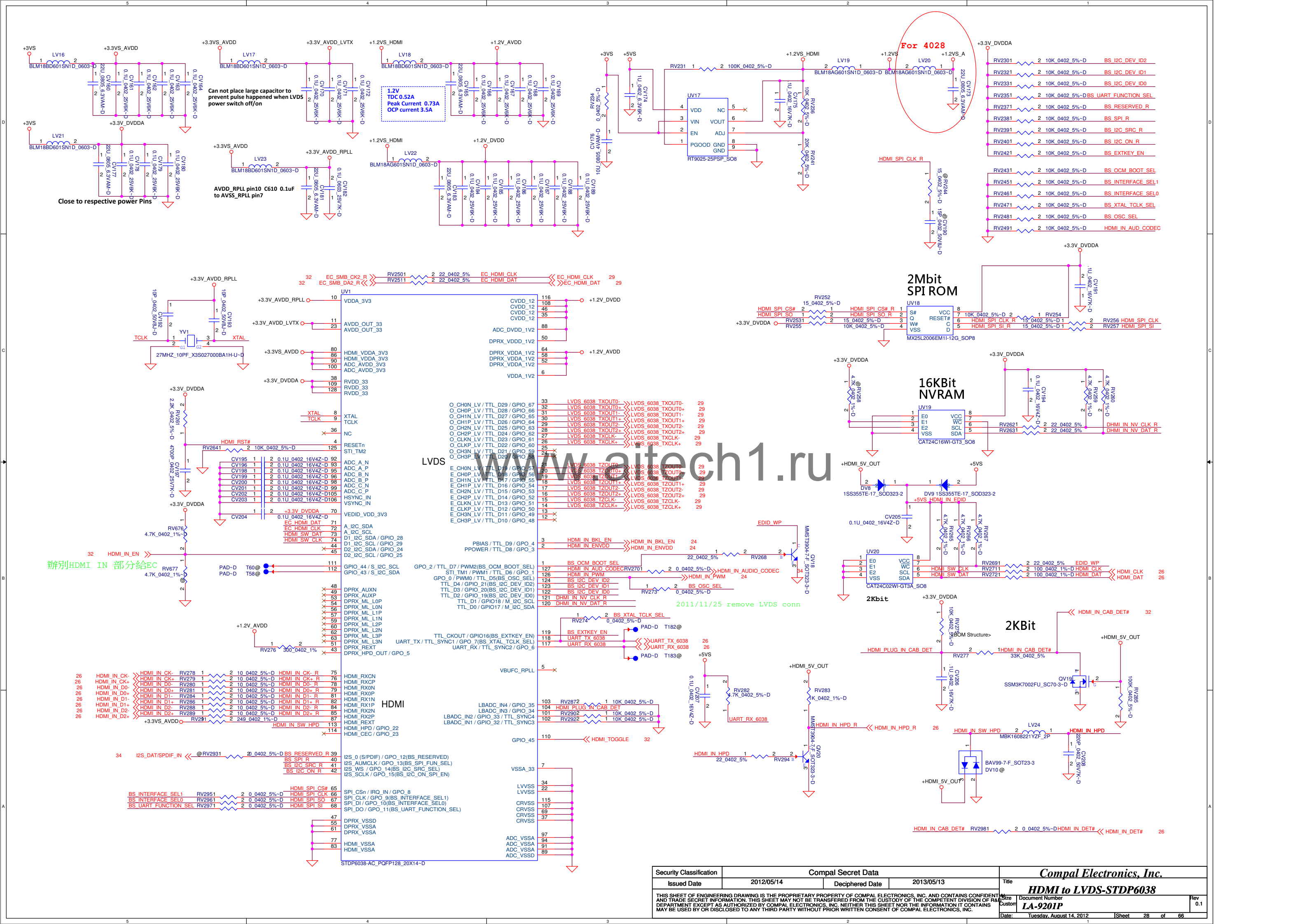
## HDMI Input/Output Connector

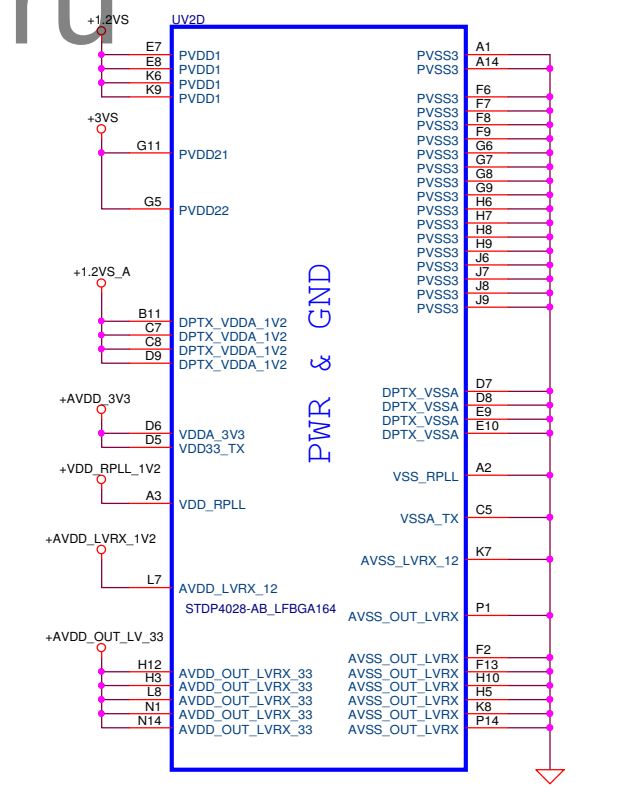
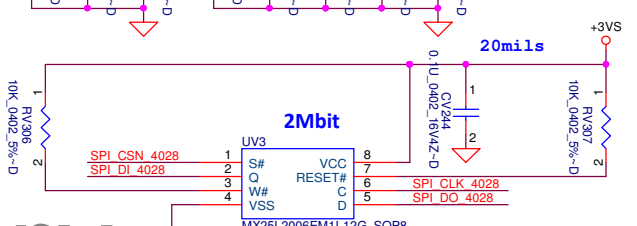
辦別HDMI IN/OUT 部分

辦別HDMI IN/OUT Cable 部分





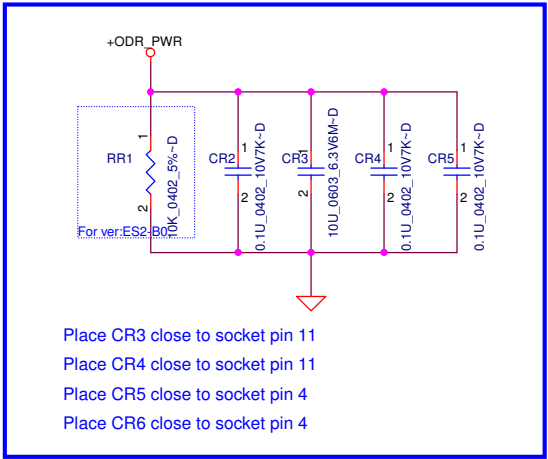
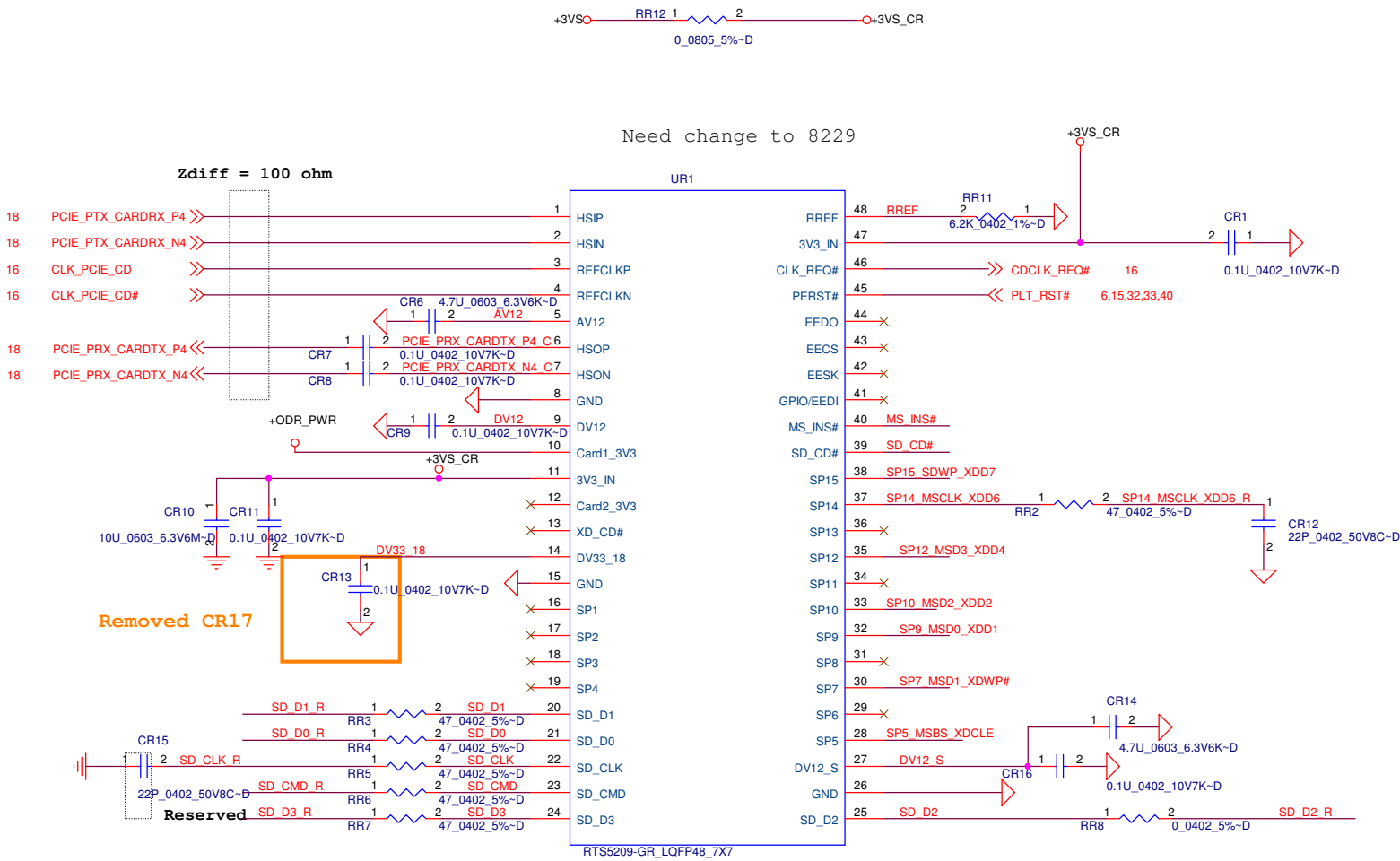




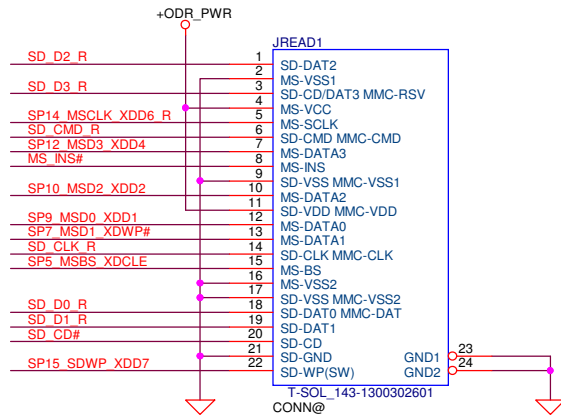
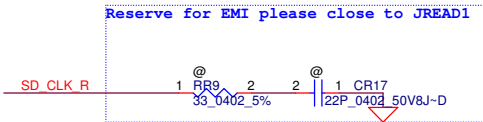
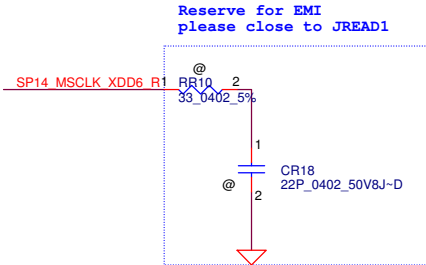
Security Classification		Compal Secret Data		<i>Compal Electronics, Inc.</i> <b>LVDS to eDP-STDP4028</b>	
Issued Date	2012/05/14	Deciphered Date	2013/05/13	Title	
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				Date:	Tuesday, August 14, 2012         Sheet 29 of 66         Rev 0.1







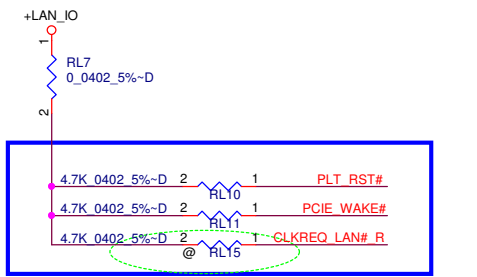
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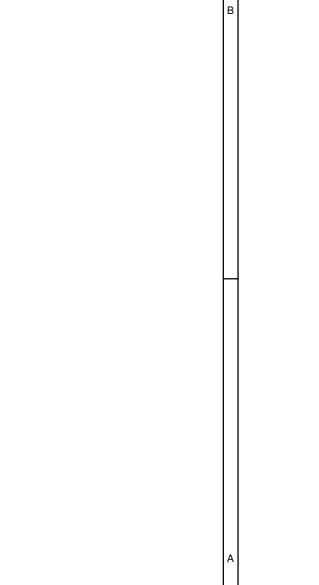
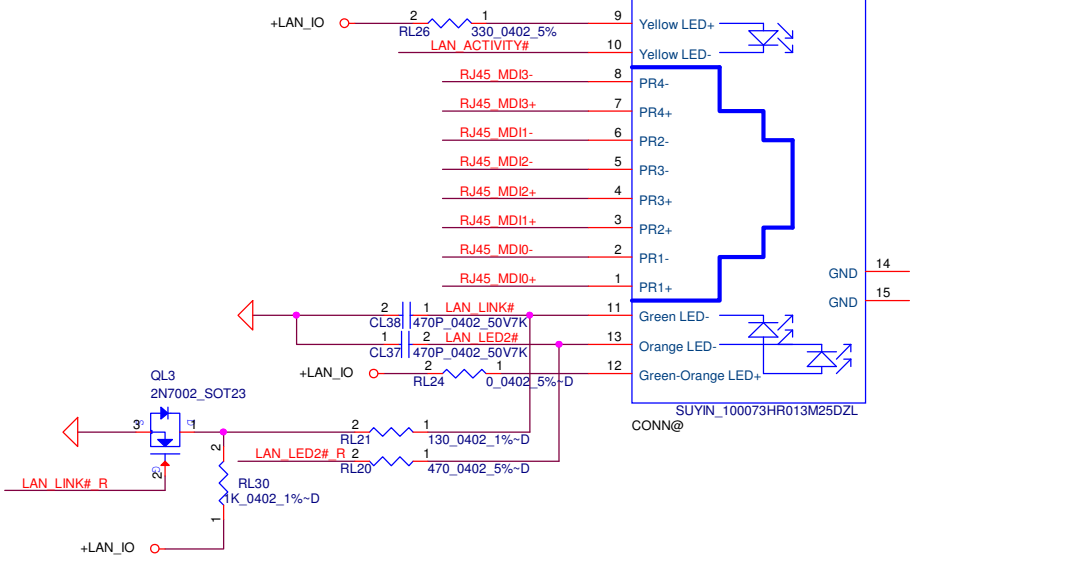
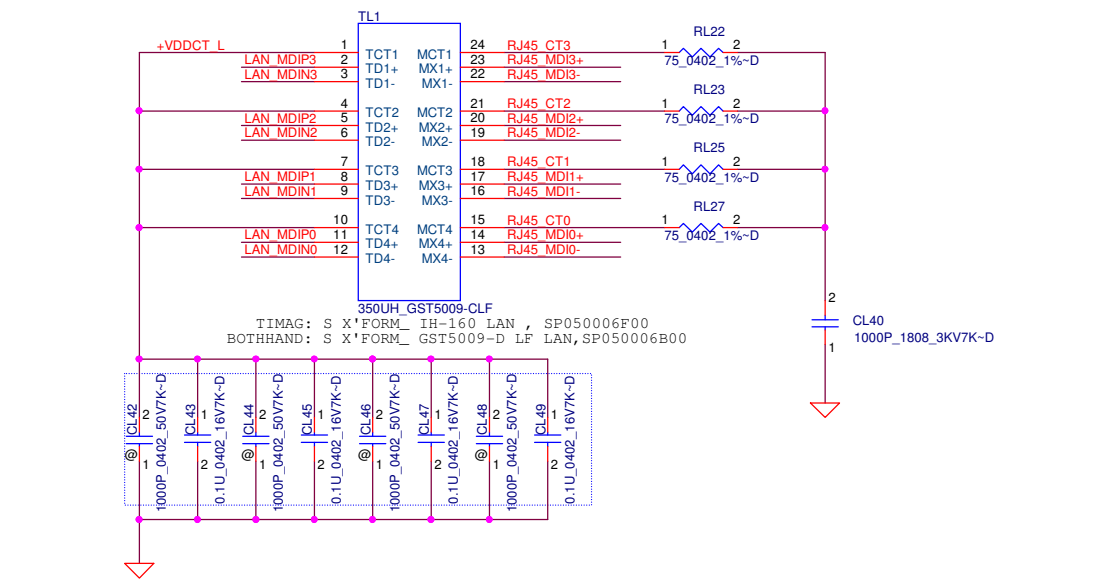
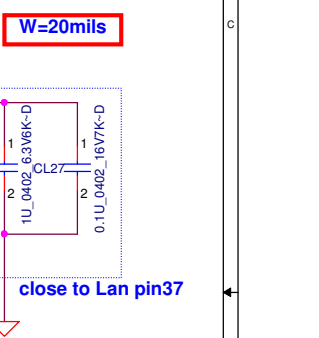
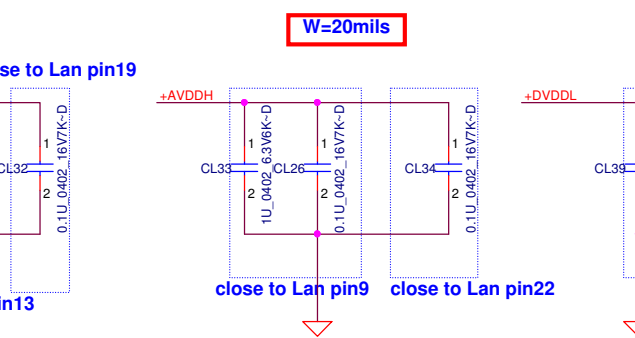
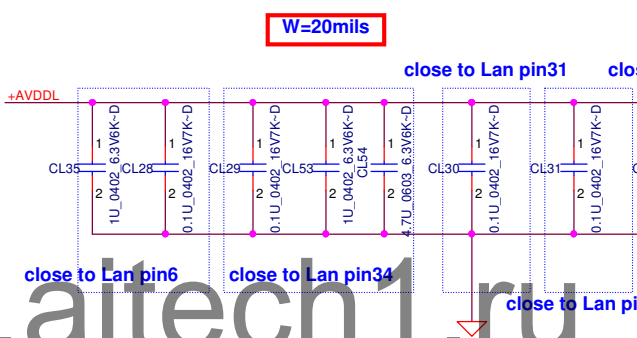
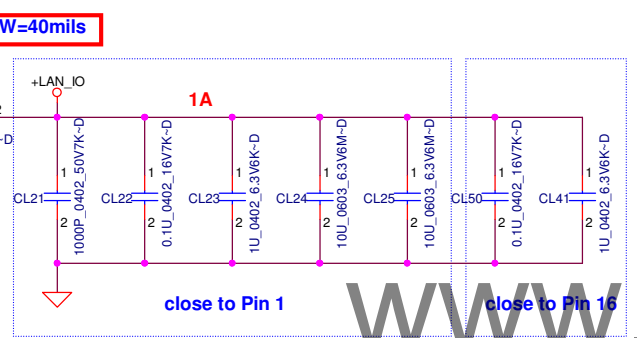
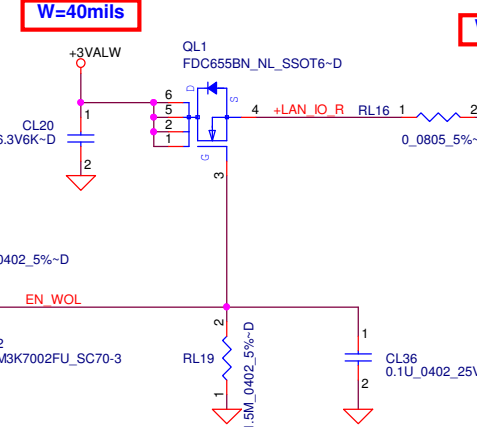
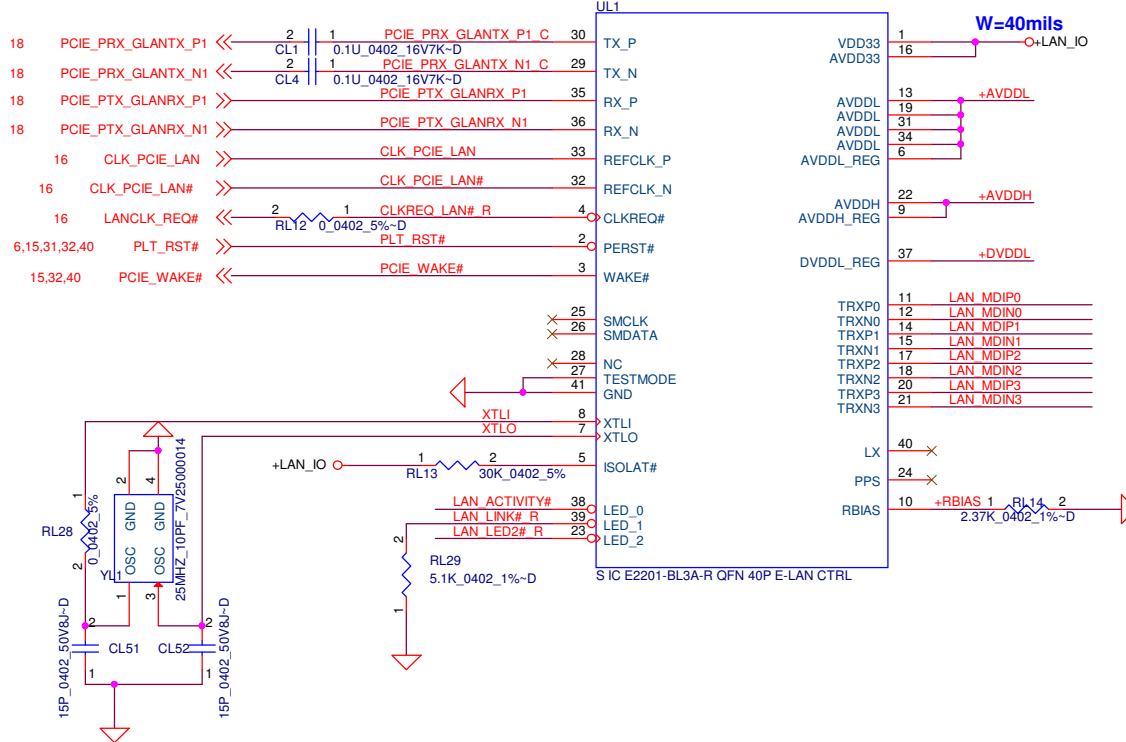
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Document Number				LA-9201P
Date: Monday, August 20, 2012				Rev 0.1
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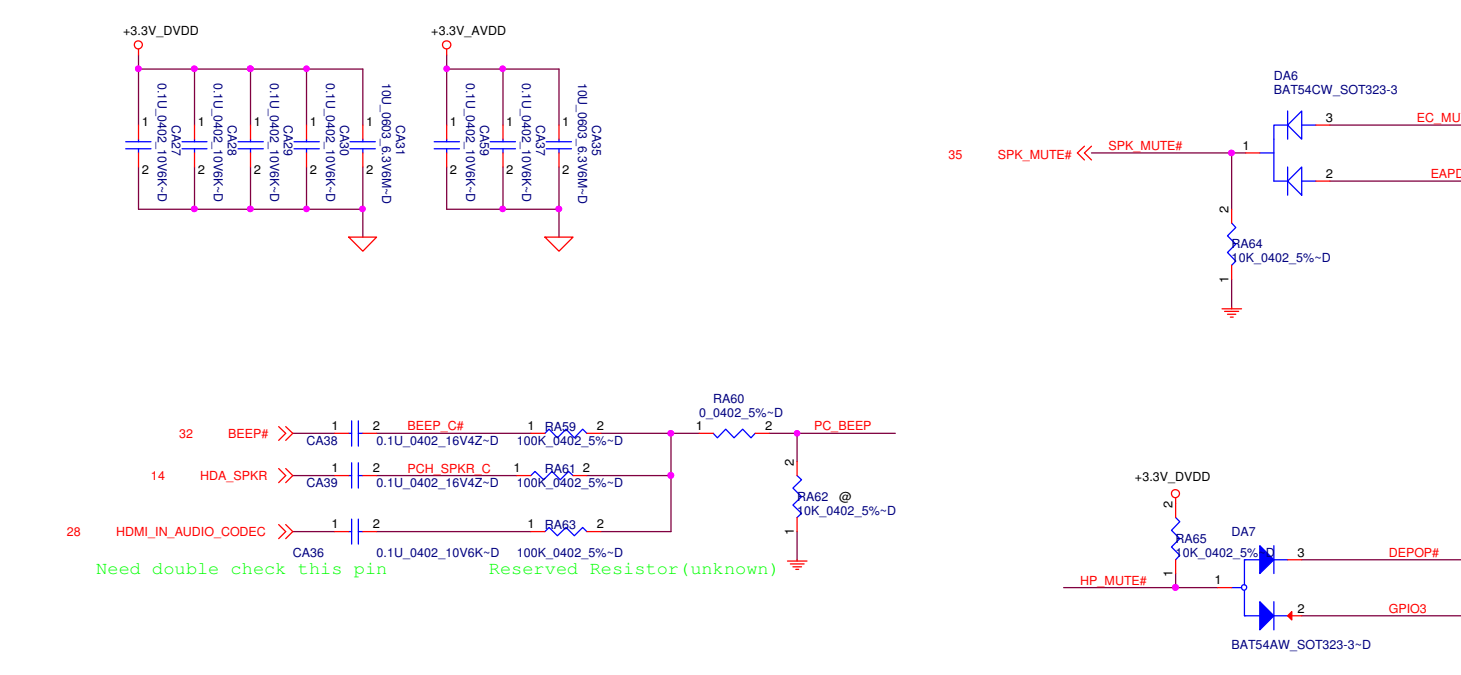
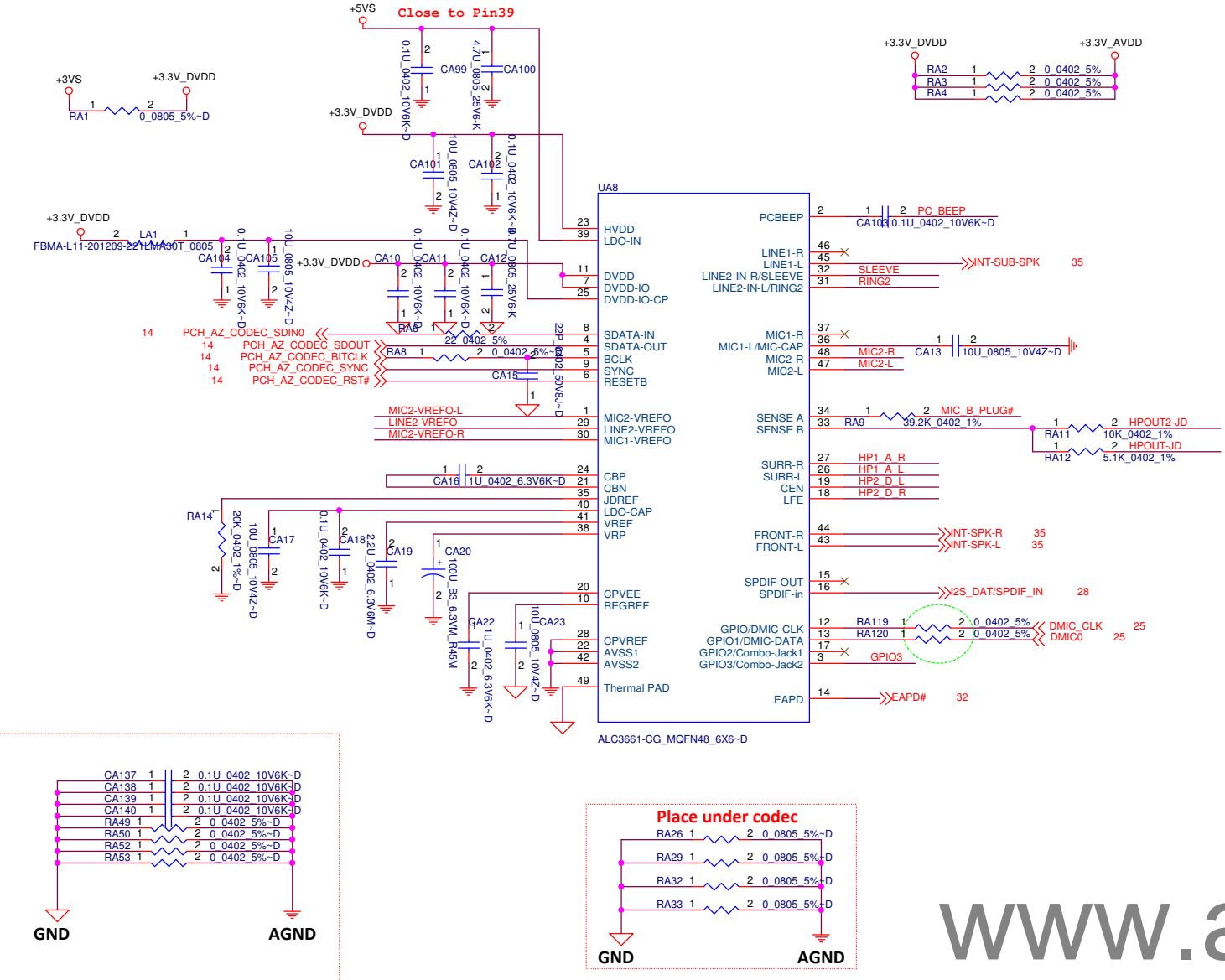




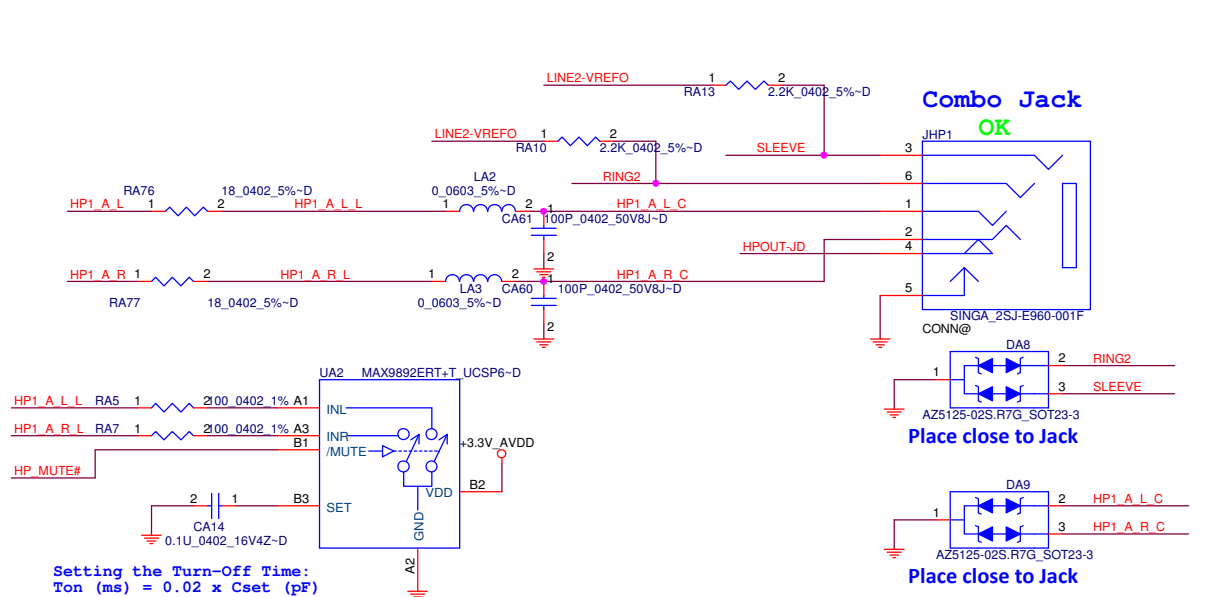
The pull-up resistors might not be necessary due to existence on PCH side.



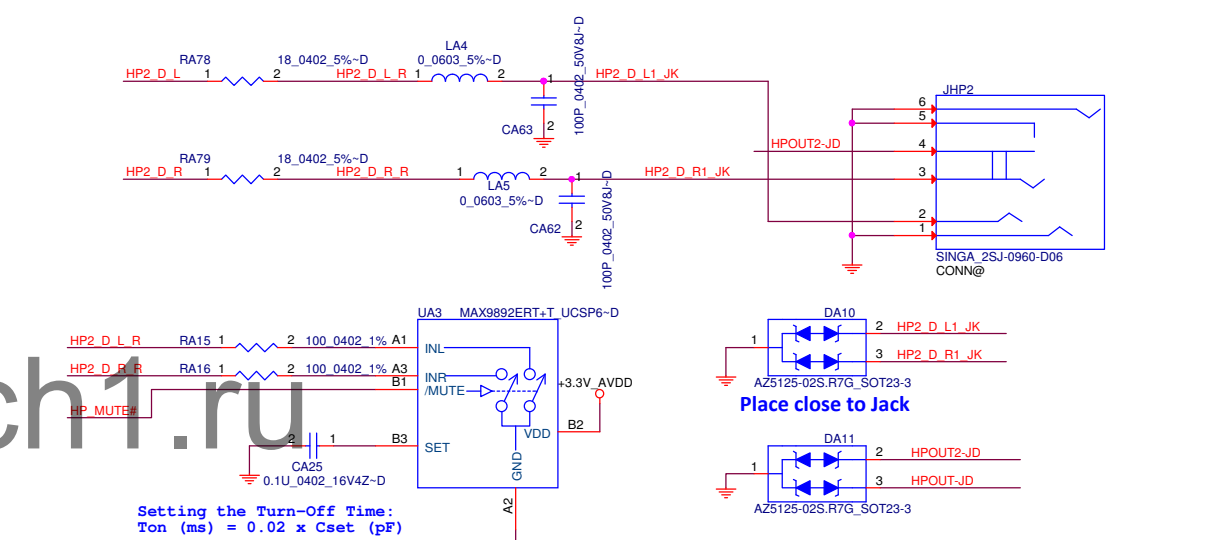
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Date: Tuesday, August 14, 2012				Sheet 33 of 66



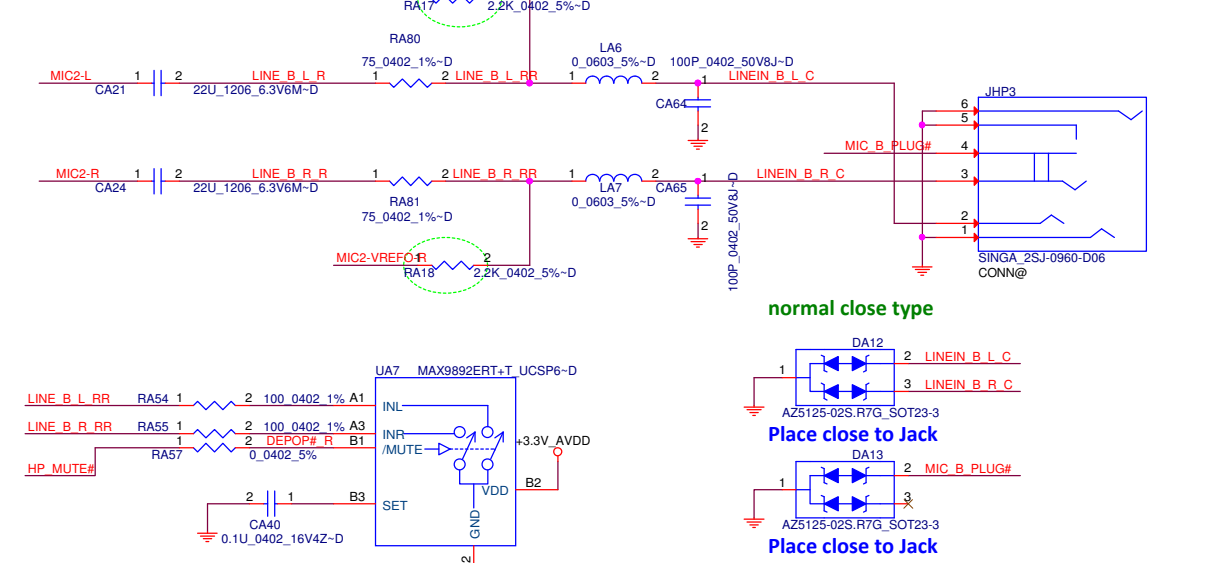
S1 (Out + In) : Front L/R + HP1 + MIC (auto-sense)



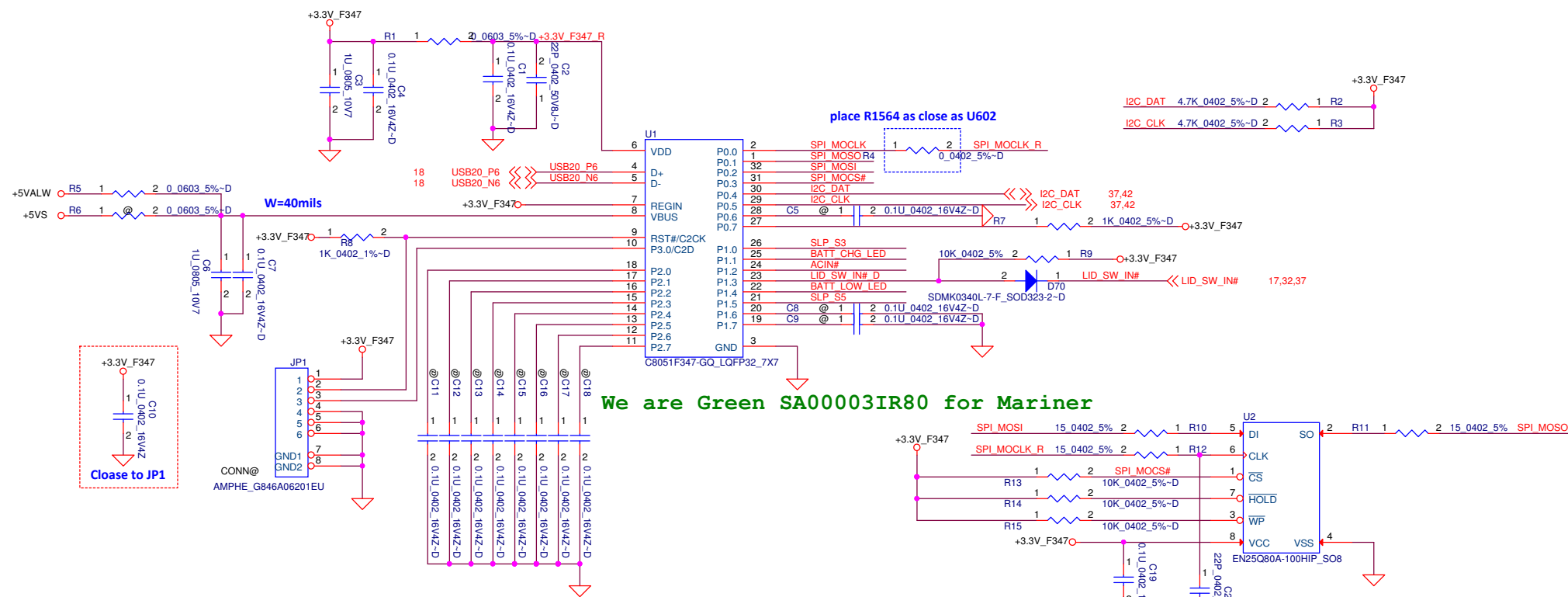
S2 (Out) :Center + HP2



S3 (Out) : Rear L/R + MIC

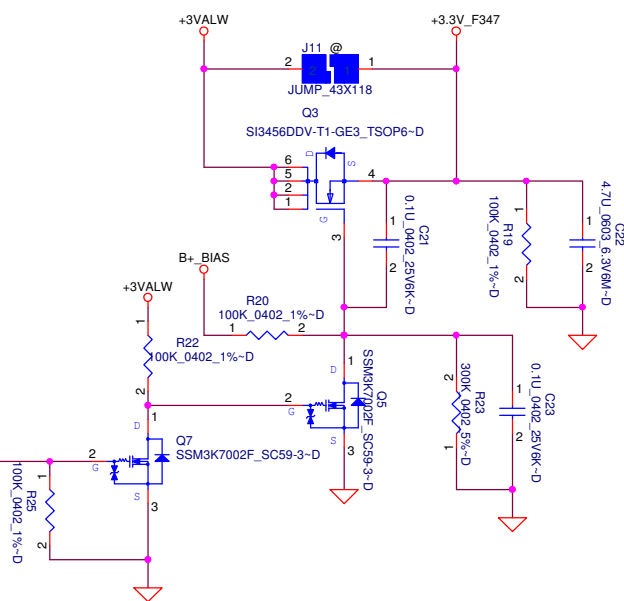
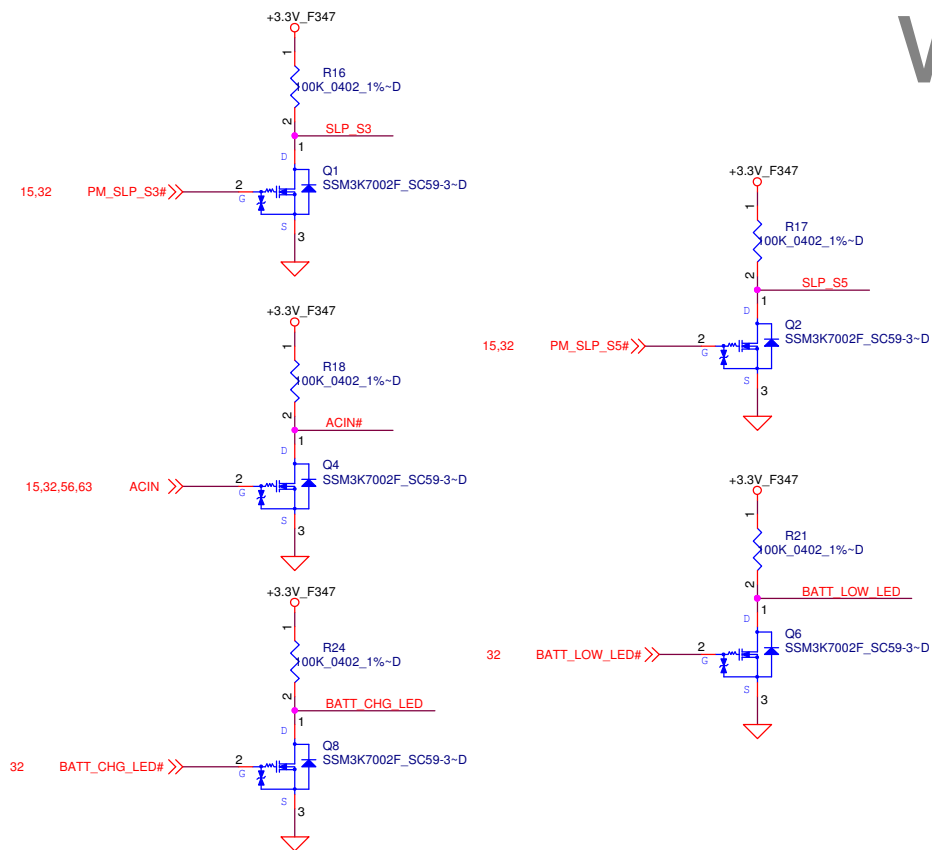






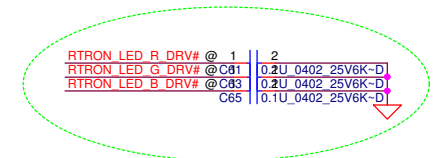
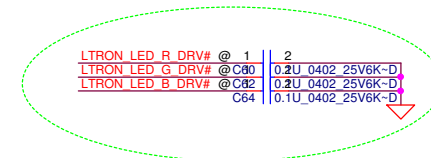
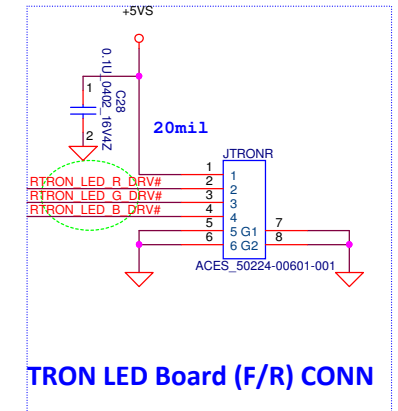
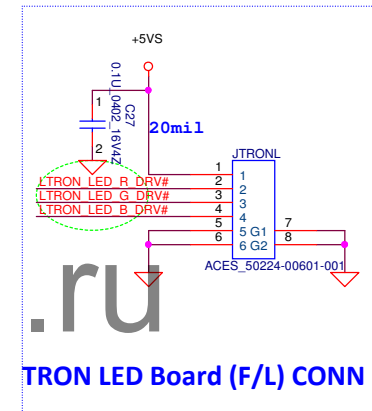
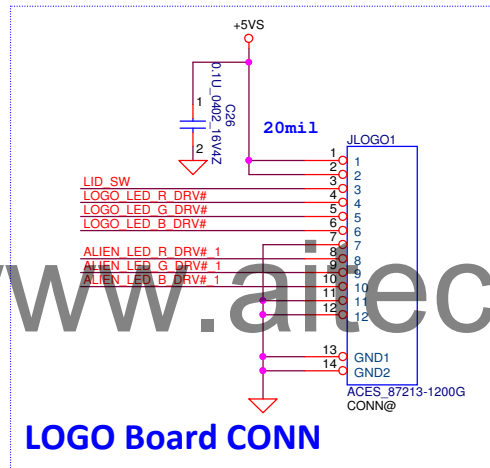
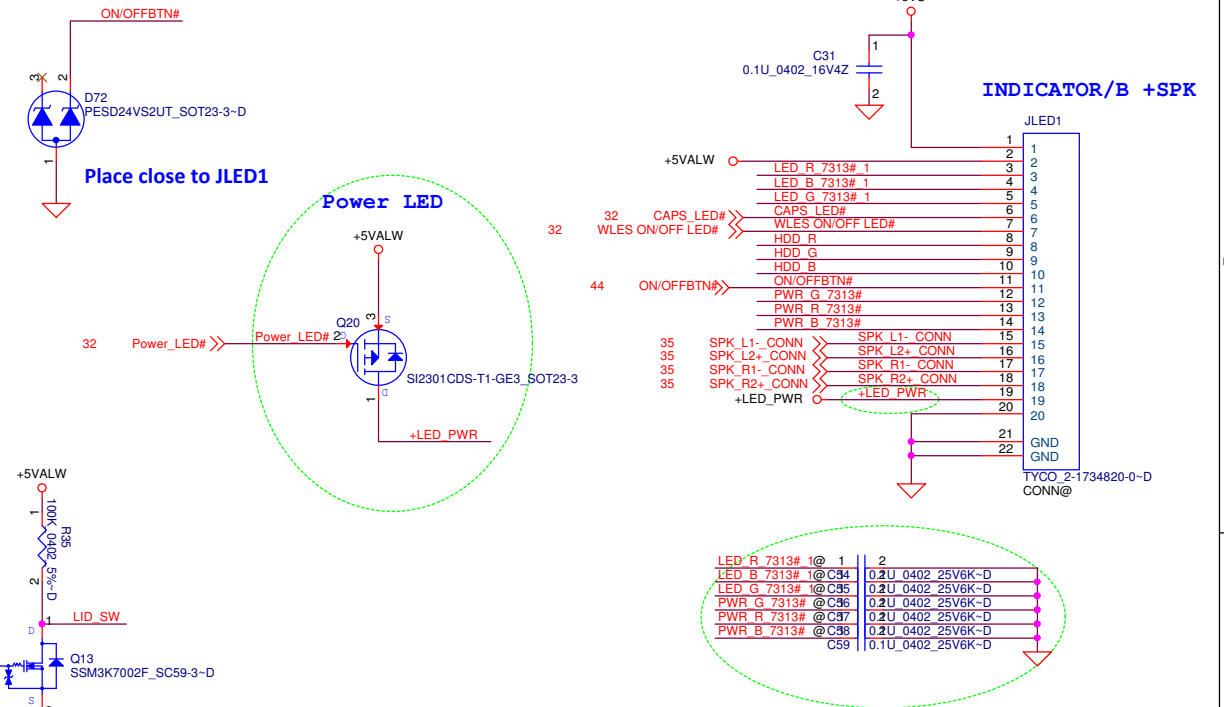
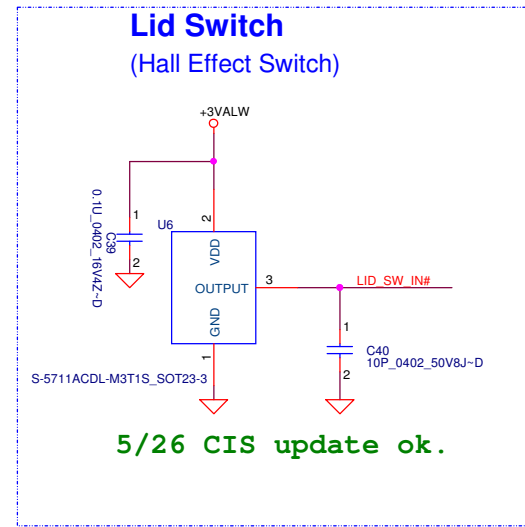
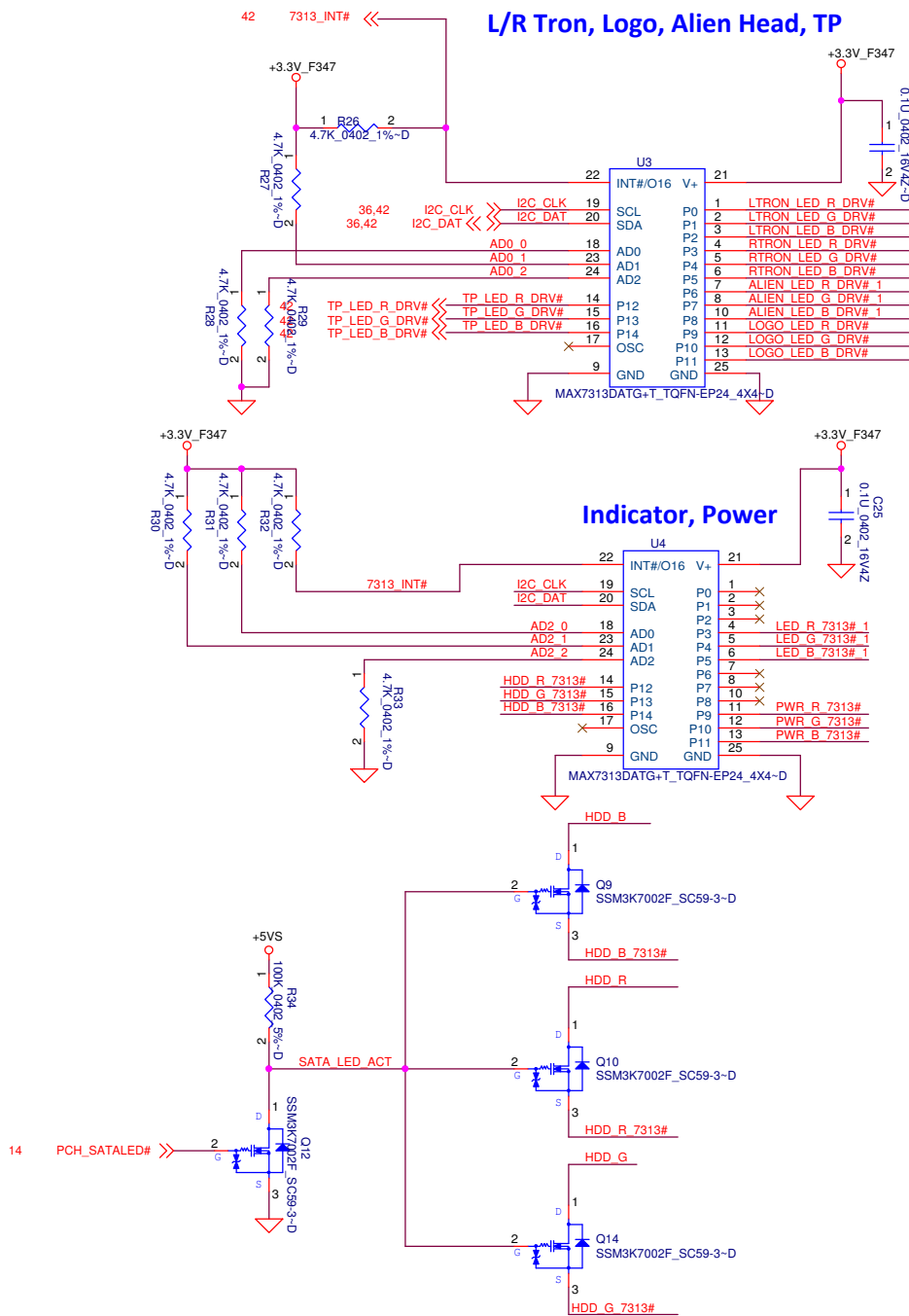
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DEVICE	MEMUS ADDRESS
MAXIM - LED	0100 000b
MAXIM - GPIO	0100 001b
I2C EEPROM	1010 000b

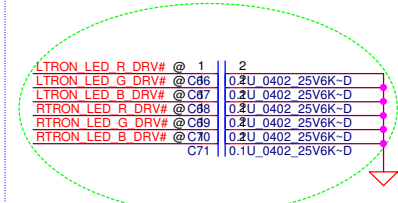
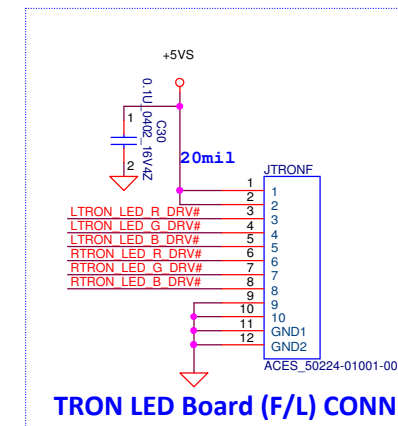
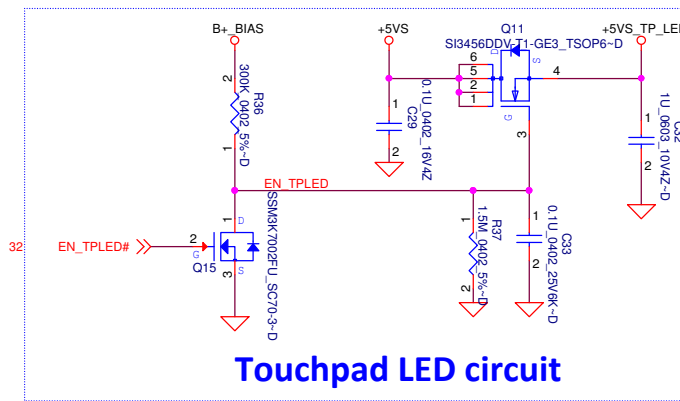
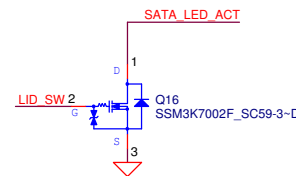


		+3.3V_F347 behavior			
		STATE			
		S0	S3	S4	S5
AC IN		ON	ON	ON	ON
BAT only		ON	ON	OFF	OFF

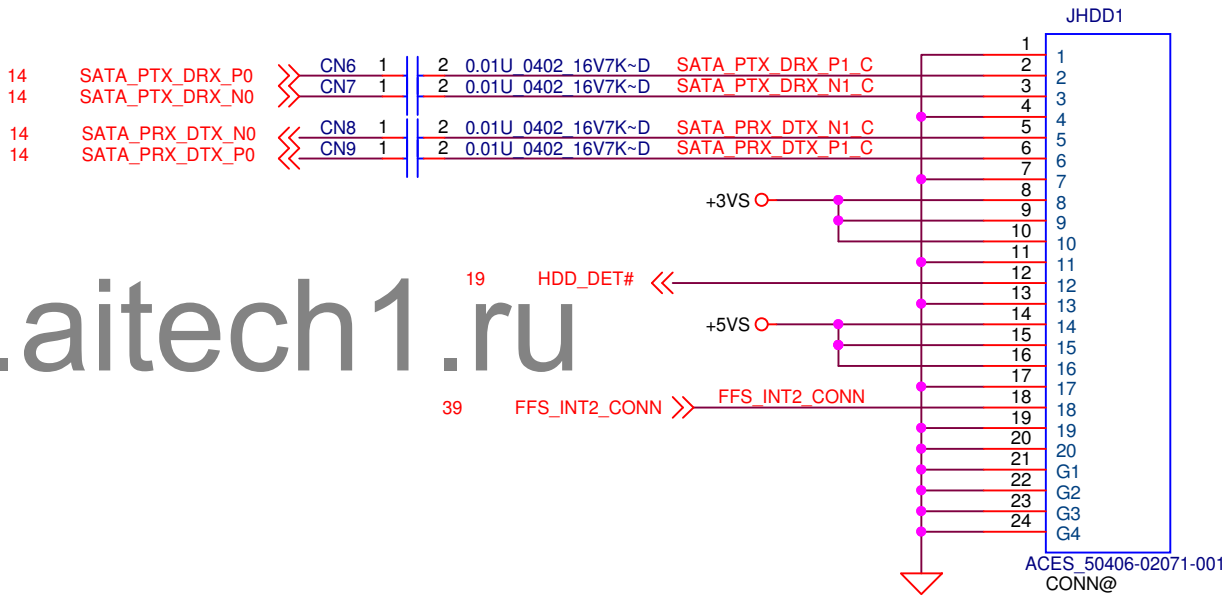
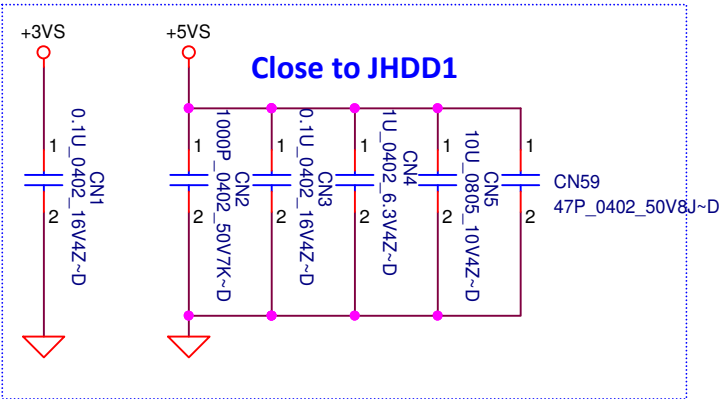
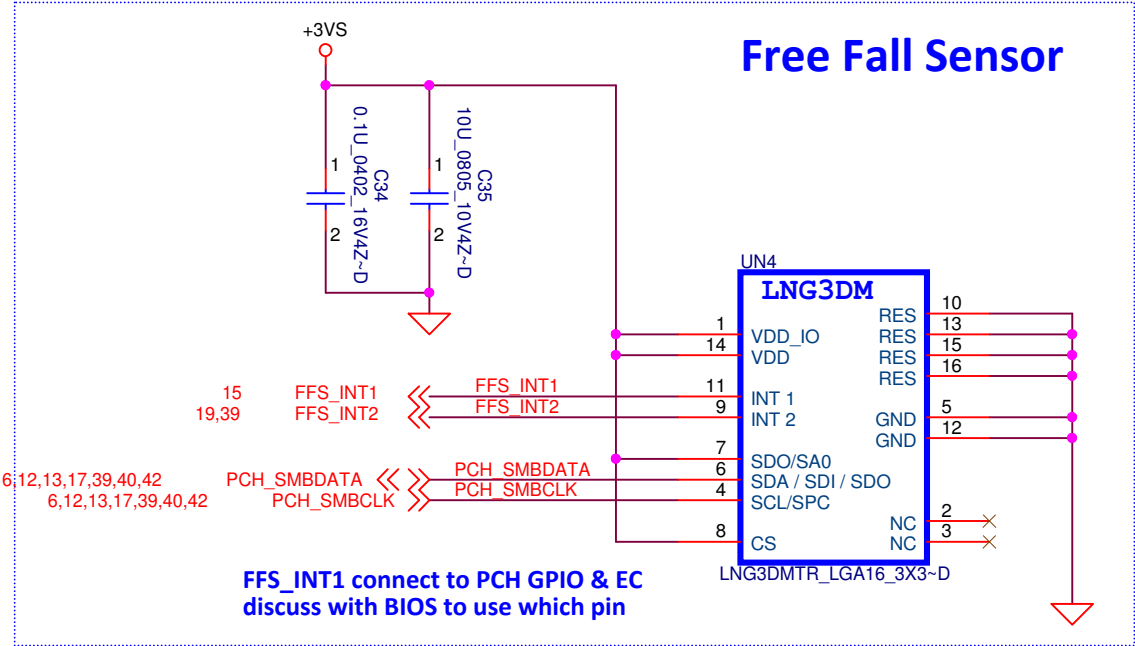
AC mode battery full in S5:turn off ELC controller



Reference	AD2	AD1	AD0	MAX7313
U605	0	1	0	Tron Lights, TP A-panel, B-Panel Logo
U608	0	1	1	Power Button, Media and Status LED Color
U?	1	0	0	Button, Indicator Brightness



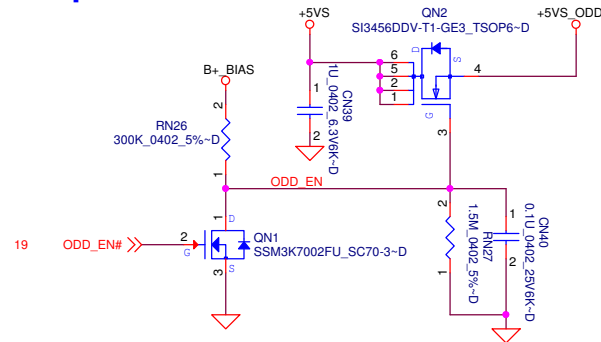




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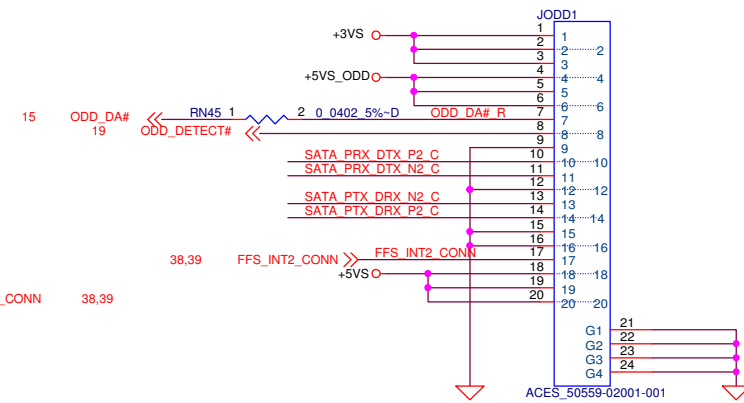
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					Document Number
					LA-9201P
					Rev 0.1
					Date: Thursday, August 16, 2012
					Sheet 38 of 66

## ODD power

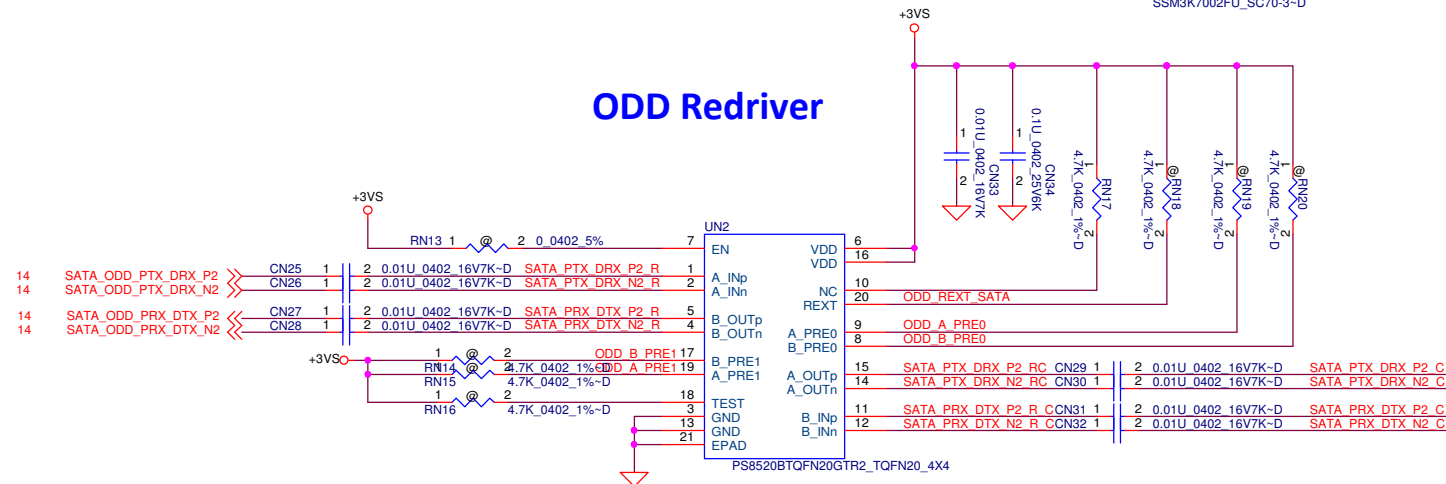


Placea caps. near ODD CONN.

## SATA ODD Conn.



## ODD Redriver



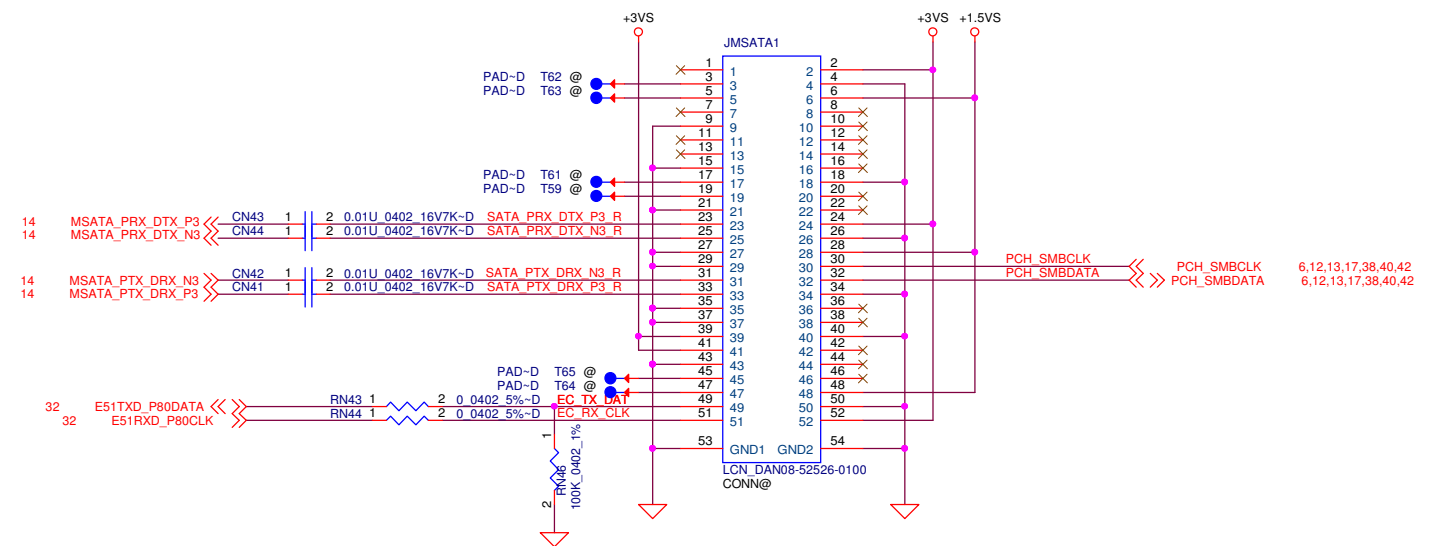
ODD\_B\_PRE0 RN21 1 @ 2 0 0402 5%  
ODD\_B\_PRE1 RN22 1 @ 2 0 0402 5%  
ODD\_A\_PRE1 RN23 1 @ 2 0 0402 5%  
ODD\_A\_PRE0 RN24 1 @ 2K 0402 5%  
ODD\_REXT\_SATA RN25 @ 5.1K 0402 1%

Pin 20:  
PARADE PS8250B:  
depop RN18, RN25  
PERICOM PI3EQX6741ST:  
pop RN18, depop RN25  
ASMEDIA ASM1466:  
pop RN18, depop RN25

Pin 9:  
PARADE PS8250B:  
depop RN24.  
PERICOM PI3EQX6741ST:  
depop RN24  
ASMEDIA ASM1466:  
pop RN24 to pull down

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## m-SATA CONN

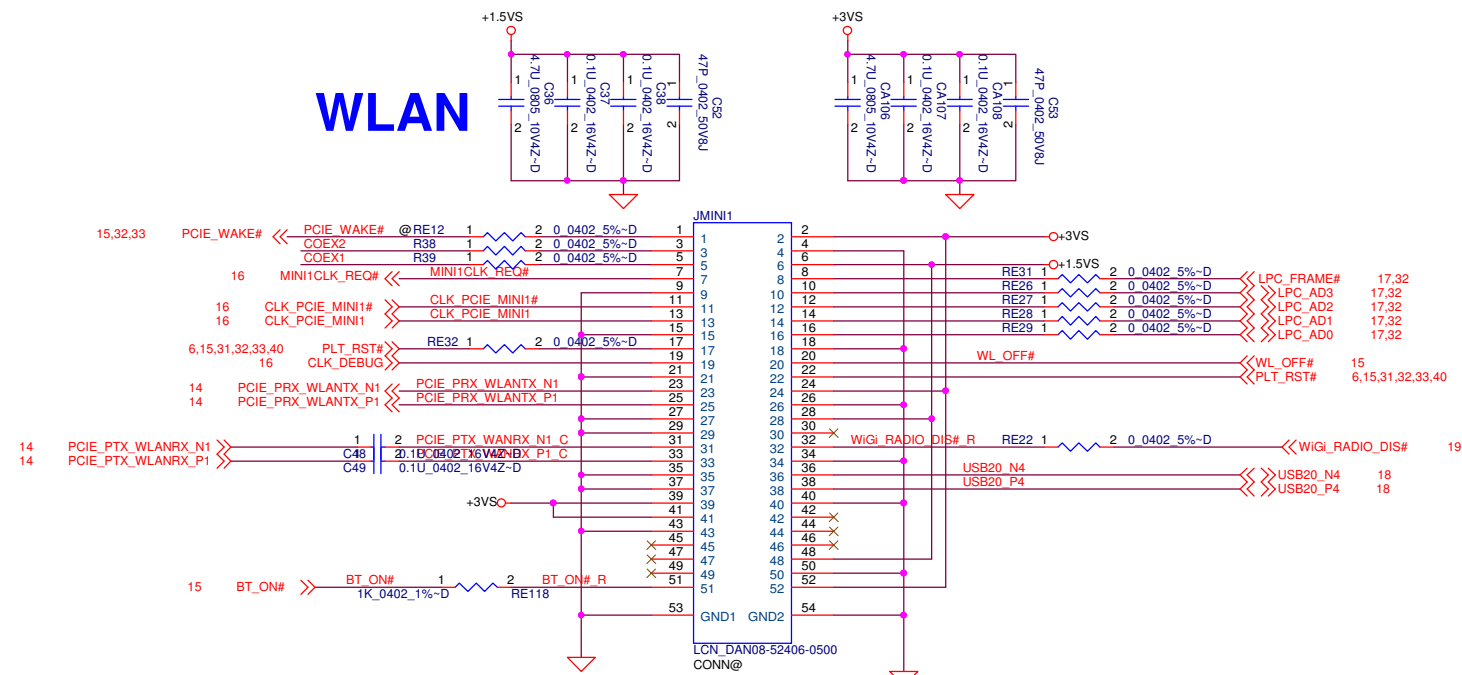


Placea caps. near JP2 CONN.

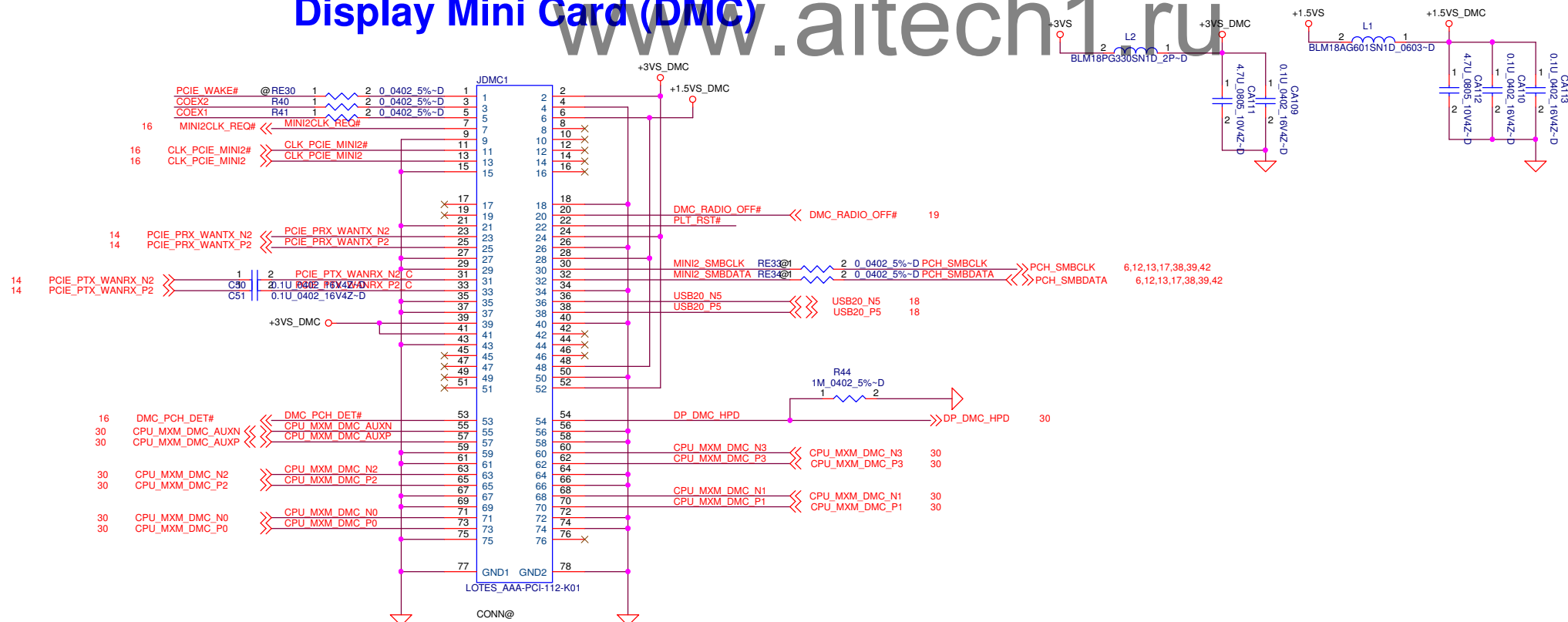
Placea caps. near JP2 CONN.

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Date: Thursday, August 16, 2012				Rev 0.1
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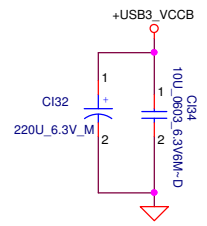
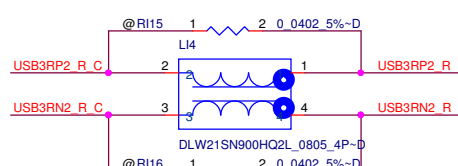
## WLAN



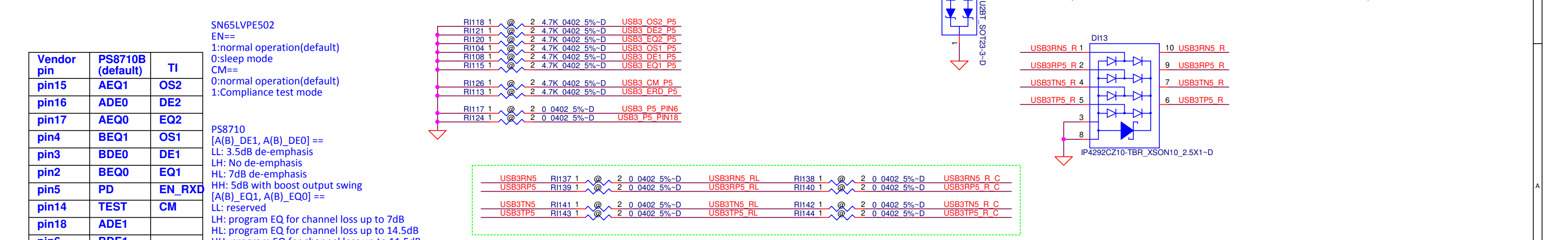
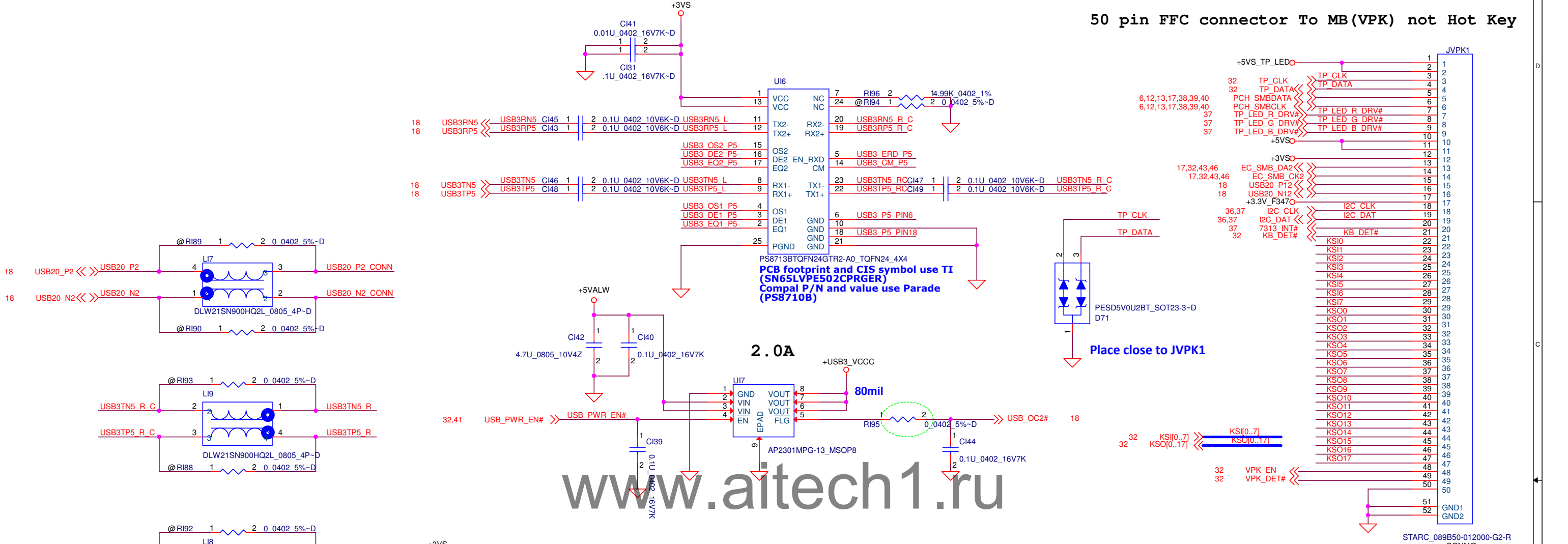
## Display Mini Card (DMC)



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Date: Thursday, August 16, 2012				Rev 0.1
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Security Classification	Compal Secret Data			<b>Compal Electronics, Inc.</b> <b>USB 3.0/2.0 x2 (left side)</b>			
Issued Date	2012/05/14	Deciphered Date	2013/05/13	Title			
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				Custm	<b>LA-9201P</b>	0.1	
				Date:	Thursday, August 16, 2012	Sheet	41 of 66



Vendor pin	PS8710B (default)	TI
pin15	AEQ1	OS2
pin16	ADE0	DE2
pin17	AEQ0	EQ2
pin4	BEQ1	OS1
pin3	BDE0	DE1
pin2	BEQ0	EQ1
pin5	PD	EN_RXD
pin14	TEST	CM
pin18	ADE1	
pin6	BDE1	

PS8710B  
EN==  
1:normal operation(default)  
0:sleep mode  
CM==  
0:normal operation(default)  
1:Compliance test mode

PS8710  
[A(B)\_DE1, A(B)\_DE0] ==  
LL: 3.5dB de-emphasis  
LH: No de-emphasis  
HL: 7dB de-emphasis  
HH: 5dB with boost output swing  
[A(B)\_EQ1, A(B)\_EQ0] ==  
LL: reserved  
LH: program EQ for channel loss up to 7dB  
HL: program EQ for channel loss up to 14.5dB  
HH: program EQ for channel loss up to 11.5dB  
TEST ==  
L: Normal operation (default)  
H: Test mode enable

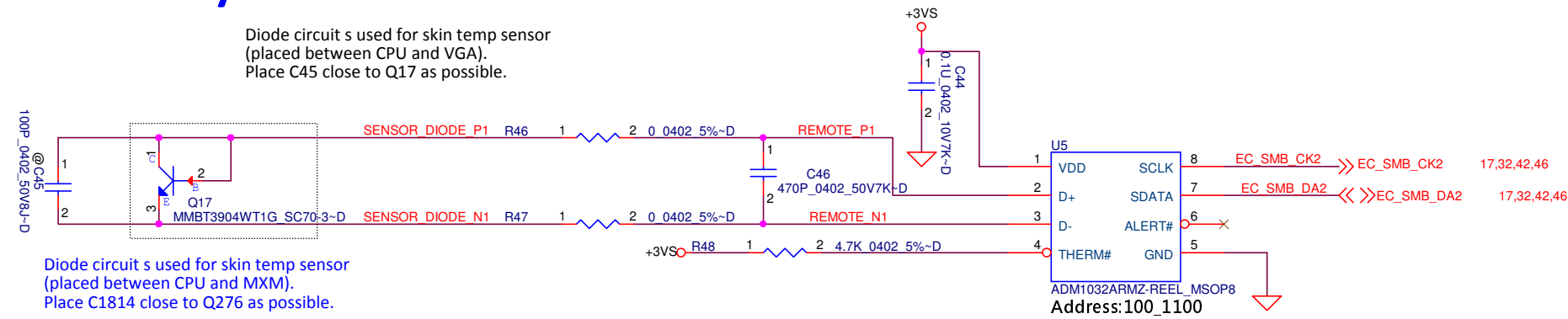
[Parade suggest]  
PS8710 AEQ0,BEQ0 adjust 7db,  
REXT use 3.3 K well get btter test result.

Security Classification		Compal Secret Data		Title	
Issued Date	2012/05/14	Deciphered Date	2013/05/13	USB & IO CONN	
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				LA-9201P	0.1
				Date: Thursday, August 16, 2012	Sheet 42 of 66

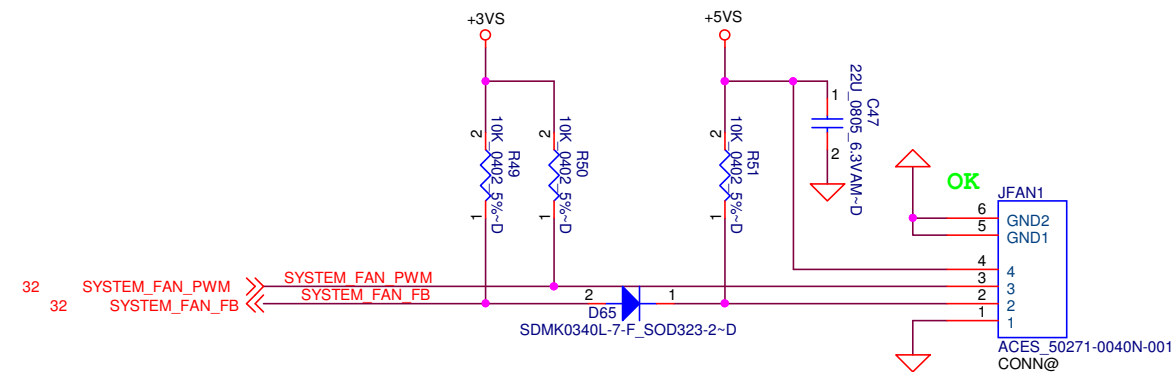


## System FAN Controller

Diode circuit s used for skin temp sensor  
(placed between CPU and VGA).  
Place C45 close to Q17 as possible.

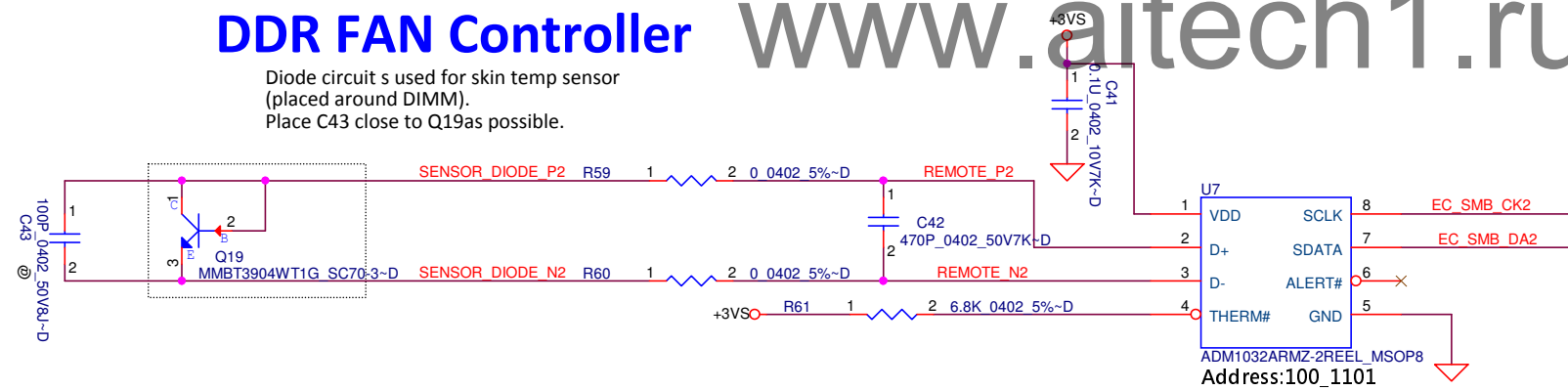


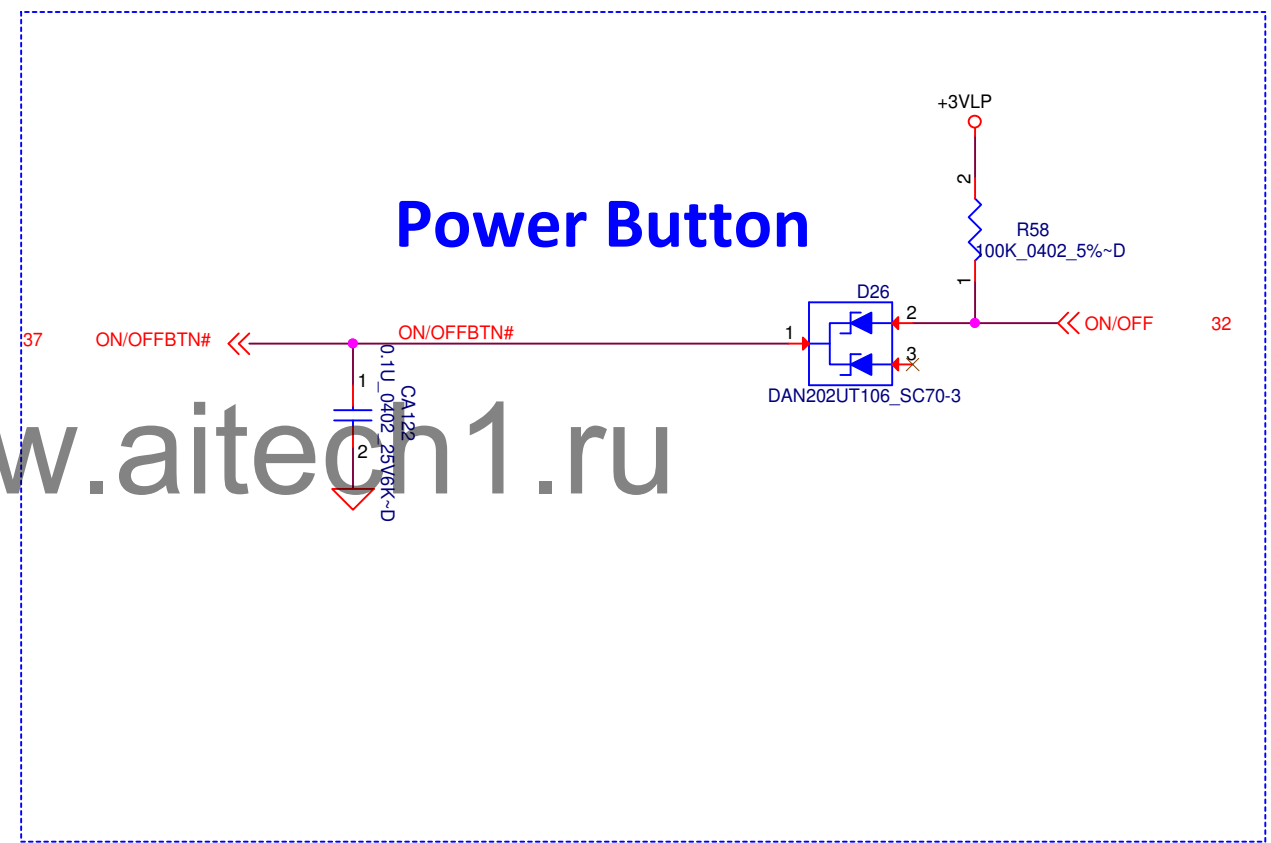
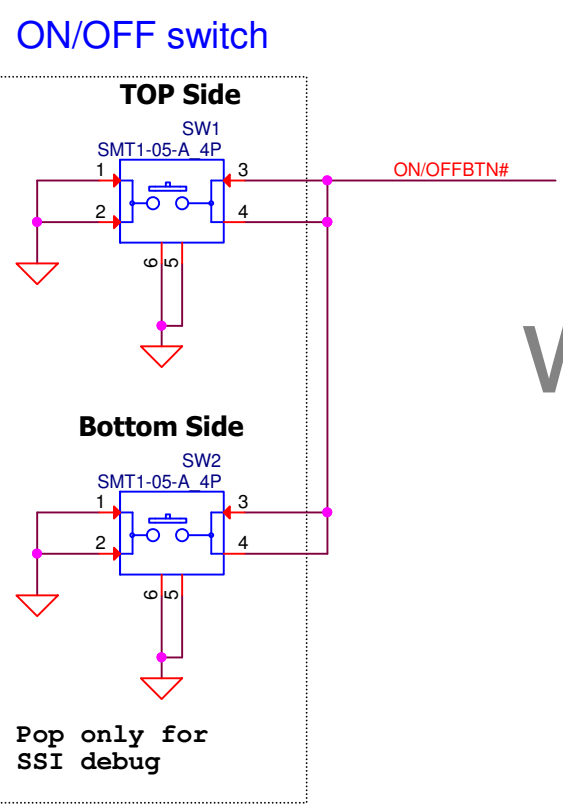
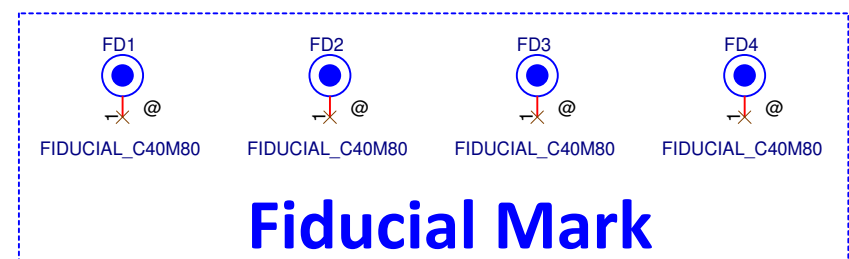
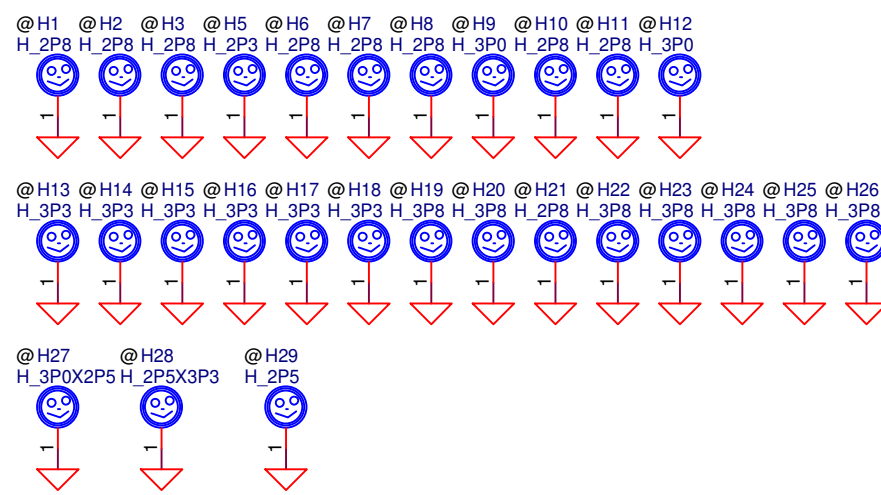
Pull up resistor on thermtrip pin	SMBUS address
4.7k	1111
6.8k	1011
10k	1001
15k	1101
22k	0011
33k	0111



## DDR FAN Controller

Diode circuit s used for skin temp sensor  
(placed around DIMM).  
Place C43 close to Q19as possible.



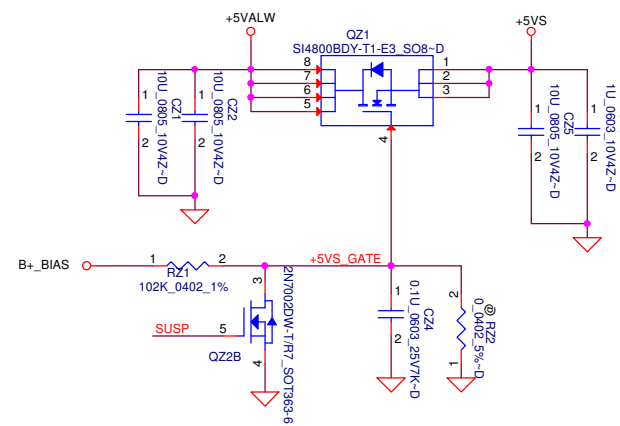


ZZZ1  
PCB-MB

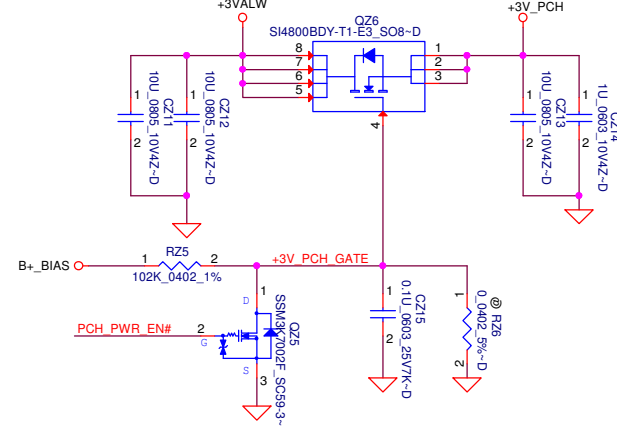
Security Classification		Compal Secret Data		Title	
Issued Date	2012/05/14	Deciphered Date	2013/05/13	KB & Power Button & IR	
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Date: Thursday, August 16, 2012		Sheet 44 of 66			

## DC to DC

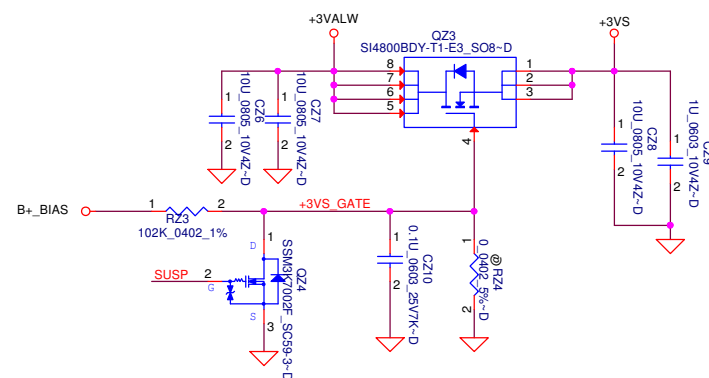
## +5VALW to +5VS



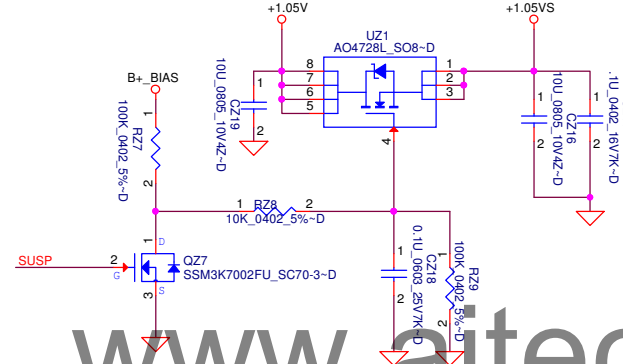
## +3VALW to +3V\_PCH



**+3VALW to +3VS**

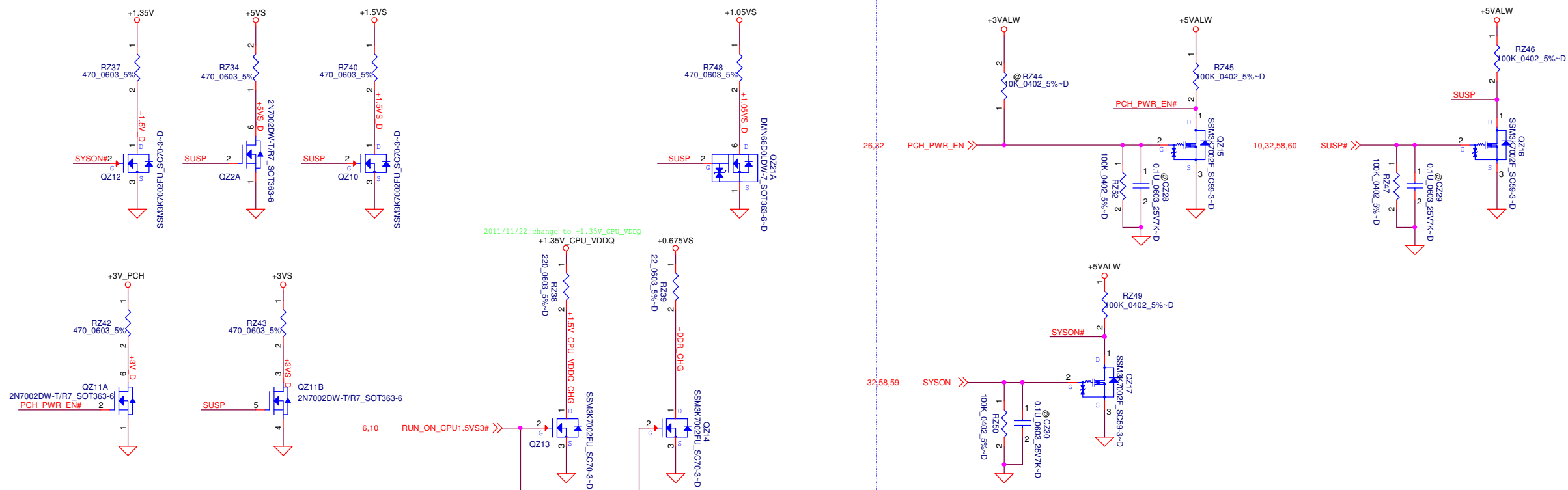


**+1.05V To +1.05VS**



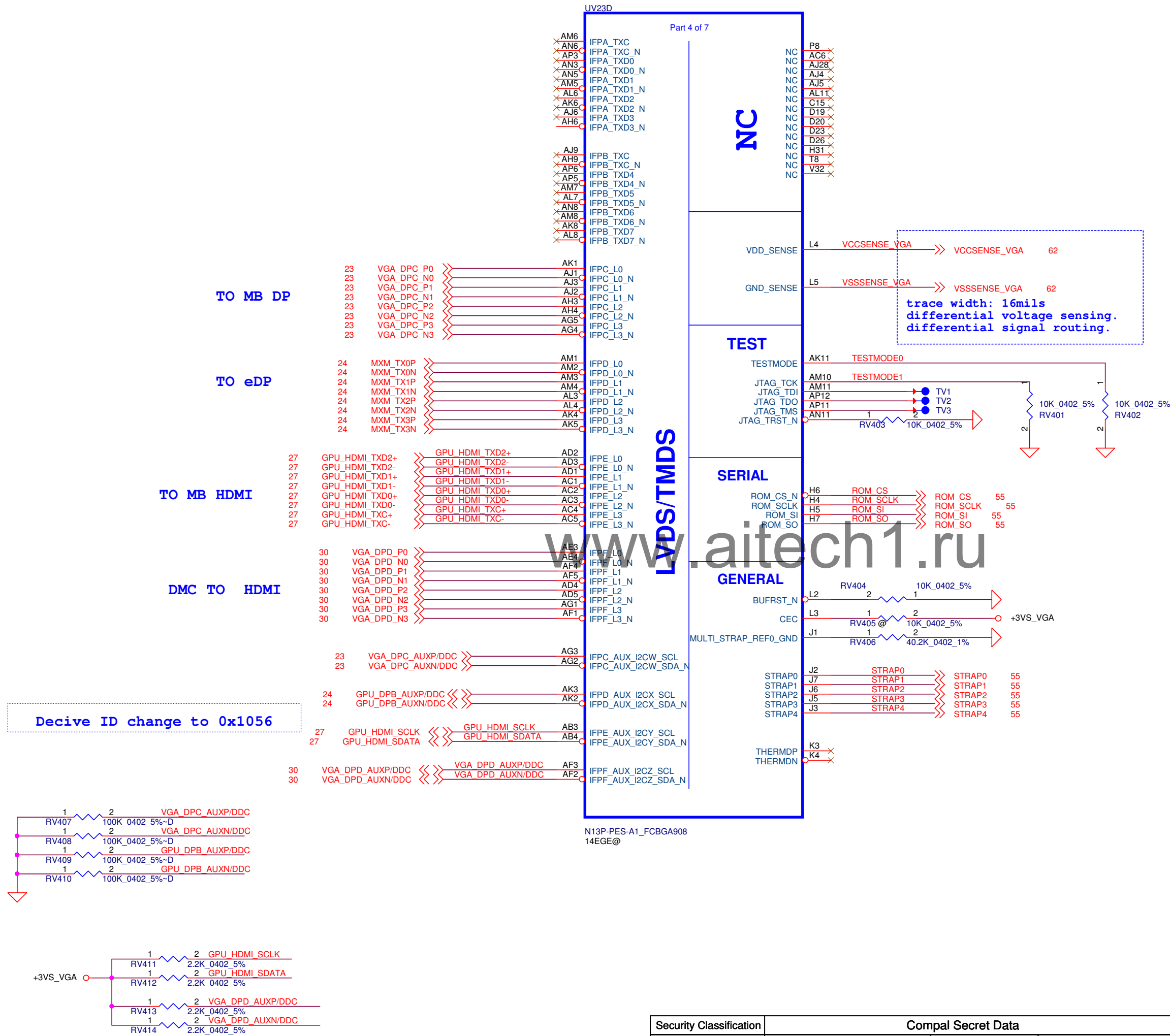
www.aitech1.ru

## Discharge Circuit



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				Custom	<i>LA-9201P</i>	0.1
Date:				Thursday, August 16, 2012	Sheet	45 of 66

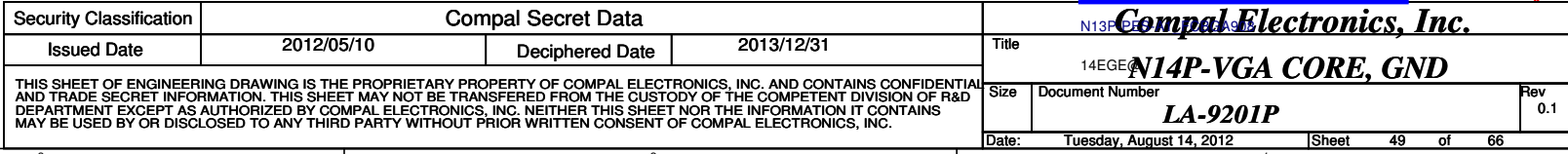


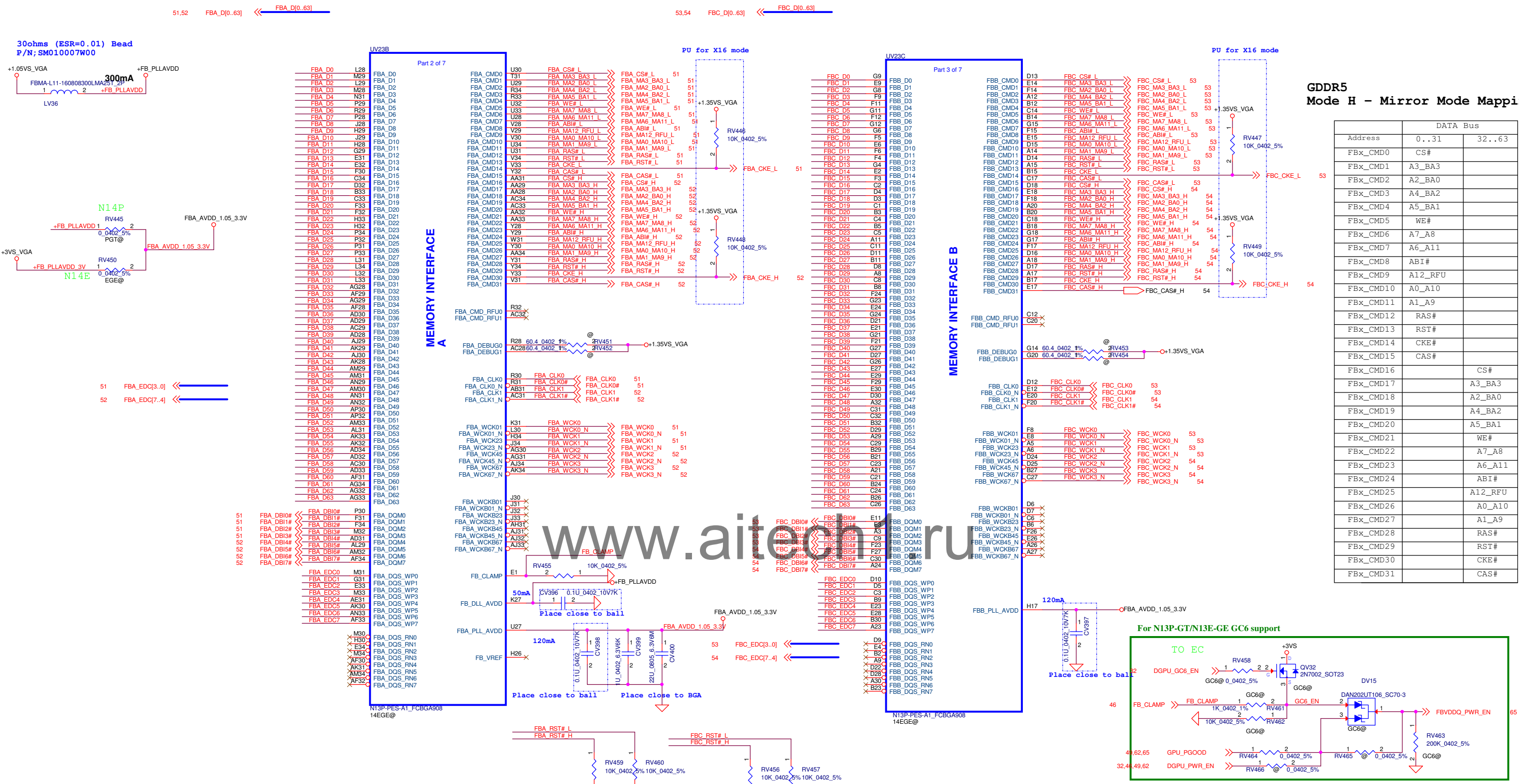


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2012/05/10		2013/12/31		2013/12/31	
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Date:		Tuesday, August 21, 2012		Sheet	
1		47		of	
66		0.1		Rev	







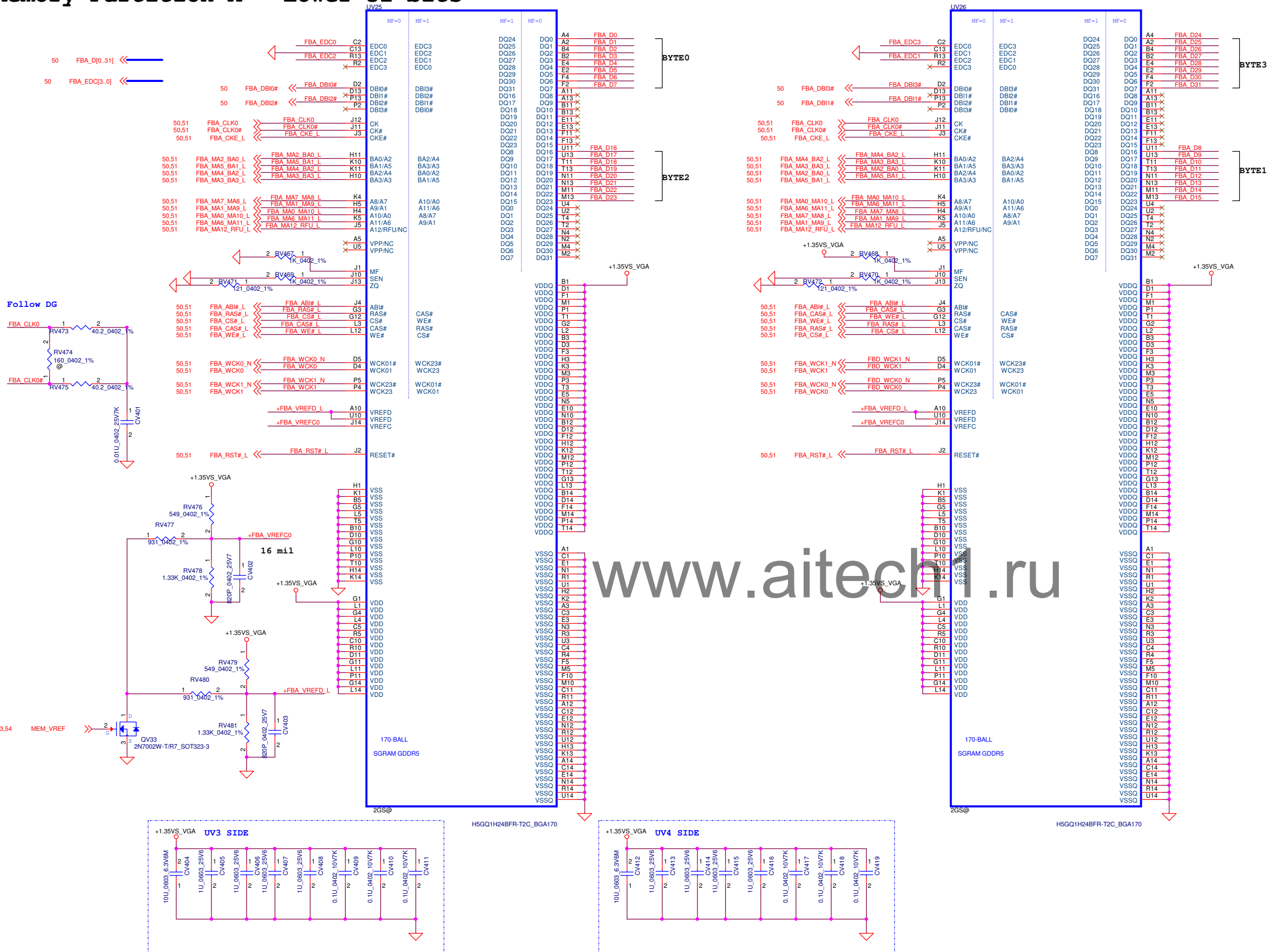


GDDR5  
Mode H - Mirror Mode Mapping

DATA Bus	
Address	0..31 32..63
FBx_CMD0	CS#
FBx_CMD1	A3_BA3
FBx_CMD2	A2_BA0
FBx_CMD3	A4_BA2
FBx_CMD4	A5_BA1
FBx_CMD5	WE#
FBx_CMD6	A7_A8
FBx_CMD7	A6_A11
FBx_CMD8	ABI#
FBx_CMD9	A12_RFU
FBx_CMD10	A0_A10
FBx_CMD11	A1_A9
FBx_CMD12	RAS#
FBx_CMD13	RST#
FBx_CMD14	CKE#
FBx_CMD15	CAS#
FBx_CMD16	CS#
FBx_CMD17	A3_BA3
FBx_CMD18	A2_BA0
FBx_CMD19	A4_BA2
FBx_CMD20	A5_BA1
FBx_CMD21	WE#
FBx_CMD22	A7_A8
FBx_CMD23	A6_A11
FBx_CMD24	ABI#
FBx_CMD25	A12_RFU
FBx_CMD26	A0_A10
FBx_CMD27	A1_A9
FBx_CMD28	RAS#
FBx_CMD29	RST#
FBx_CMD30	CKE#
FBx_CMD31	CAS#



### Memory Partition A - Lower 32 bits

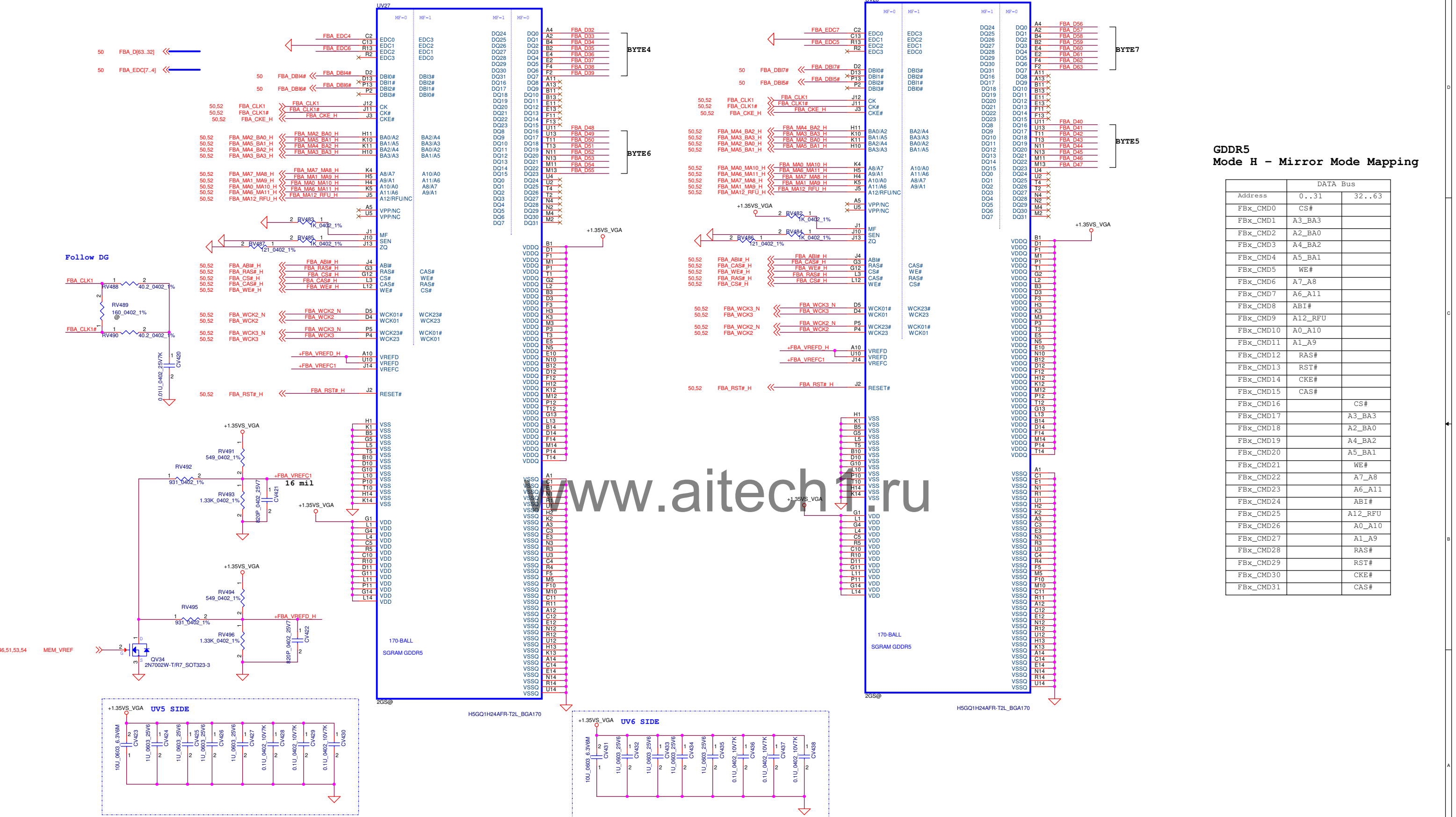


## GDDR5

### Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FbX_CMD0	CS#	
FbX_CMD1	A3_BA3	
FbX_CMD2	A2_BA0	
FbX_CMD3	A4_BA2	
FbX_CMD4	A5_BA1	
FbX_CMD5	WE#	
FbX_CMD6	A7_A8	
FbX_CMD7	A6_A11	
FbX_CMD8	ABI#	
FbX_CMD9	A12_RFU	
FbX_CMD10	A0_A10	
FbX_CMD11	A1_A9	
FbX_CMD12	RAS#	
FbX_CMD13	RST#	
FbX_CMD14	CKE#	
FbX_CMD15	CAS#	
FbX_CMD16		CS#
FbX_CMD17		A3_BA3
FbX_CMD18		A2_BA0
FbX_CMD19		A4_BA2
FbX_CMD20		A5_BA1
FbX_CMD21		WE#
FbX_CMD22		A7_A8
FbX_CMD23		A6_A11
FbX_CMD24		ABI#
FbX_CMD25		A12_RFU
FbX_CMD26		A0_A10
FbX_CMD27		A1_A9
FbX_CMD28		RAS#
FbX_CMD29		RST#
FbX_CMD30		CKE#
FbX_CMD31		CAS#

Memory Partition A - Upper 32 bits

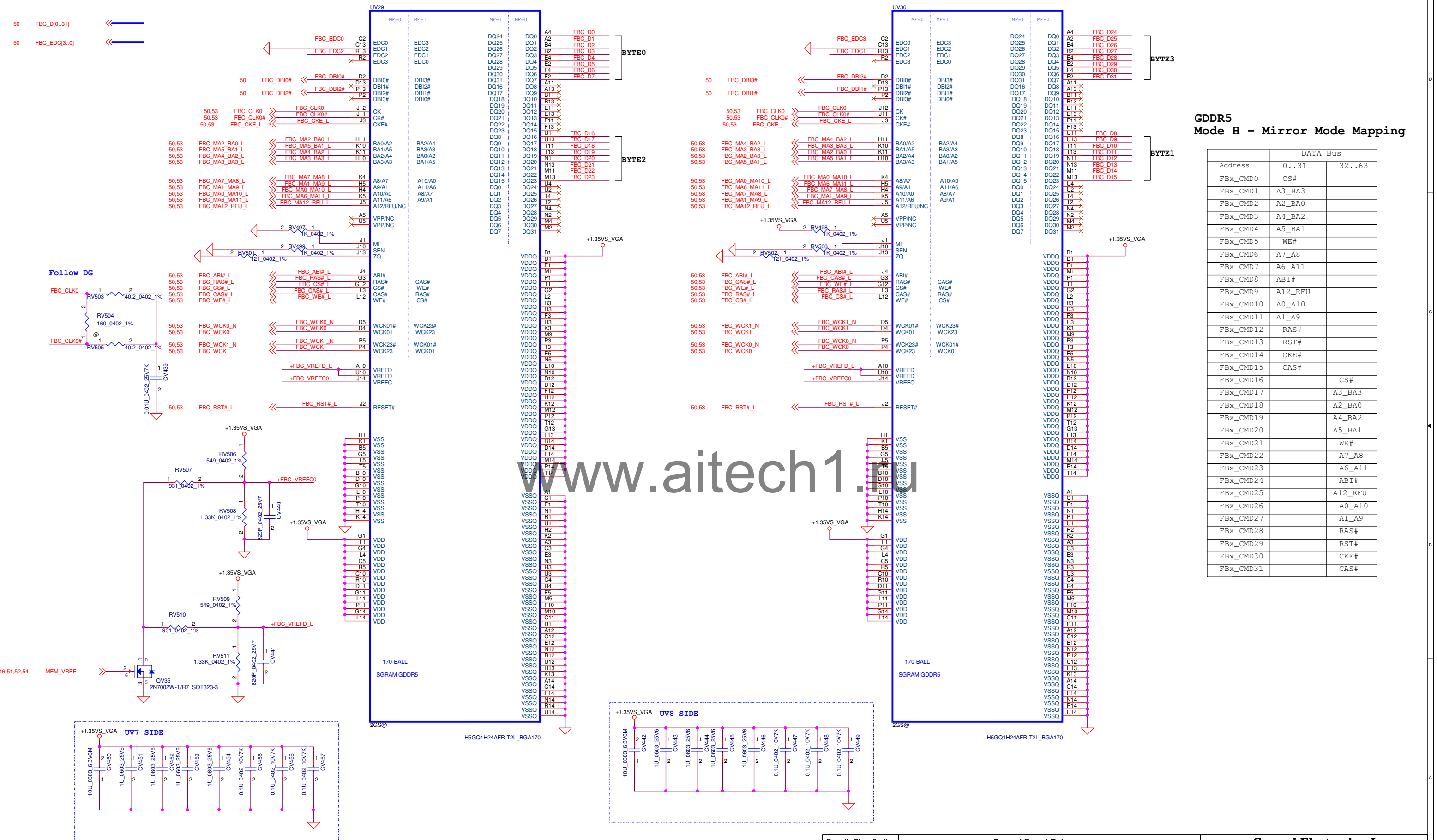


GDDR5  
Mode H - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	AB1#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		AB1#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#



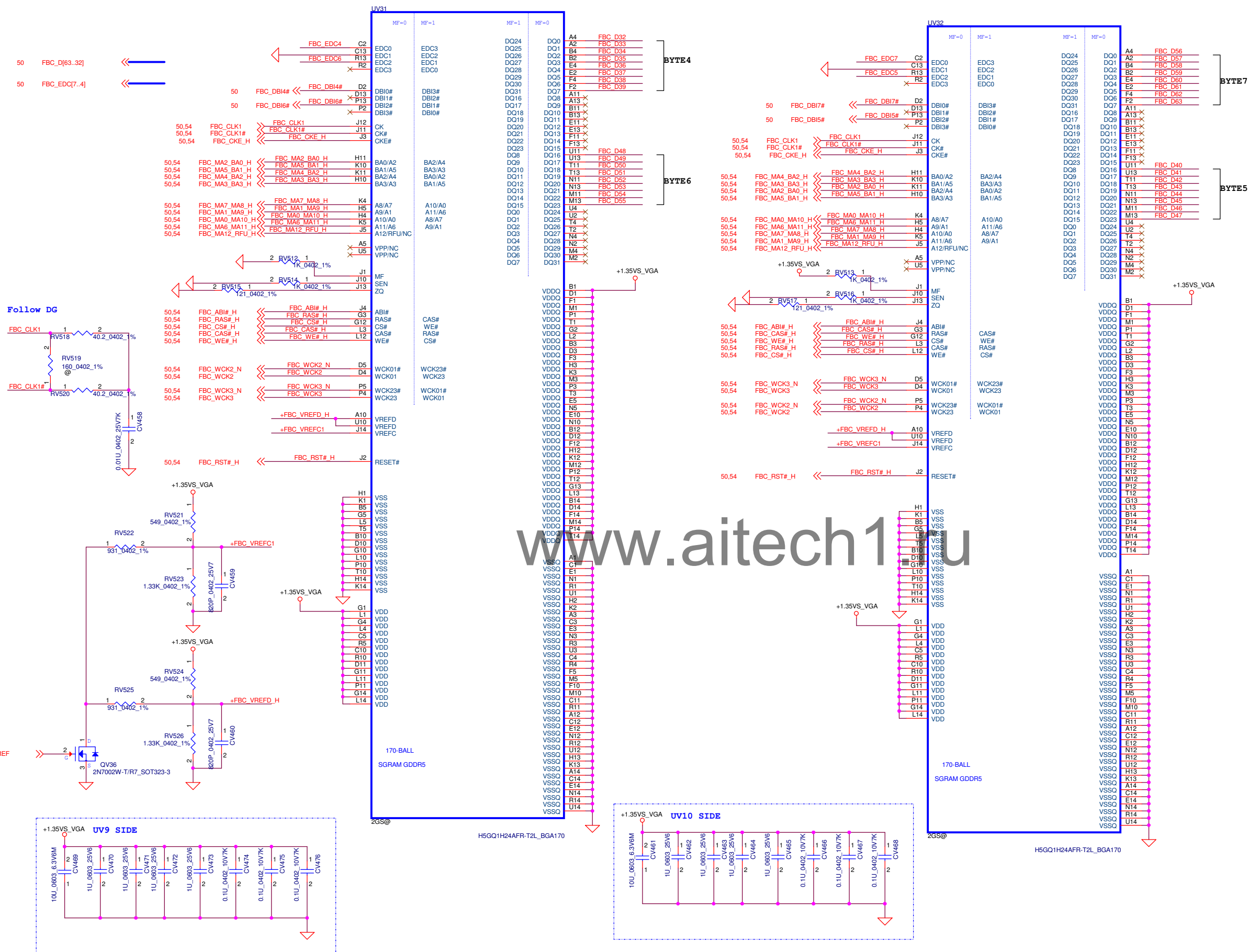
Memory Partition C - Lower 32 bits



GDDR5 Mode H - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

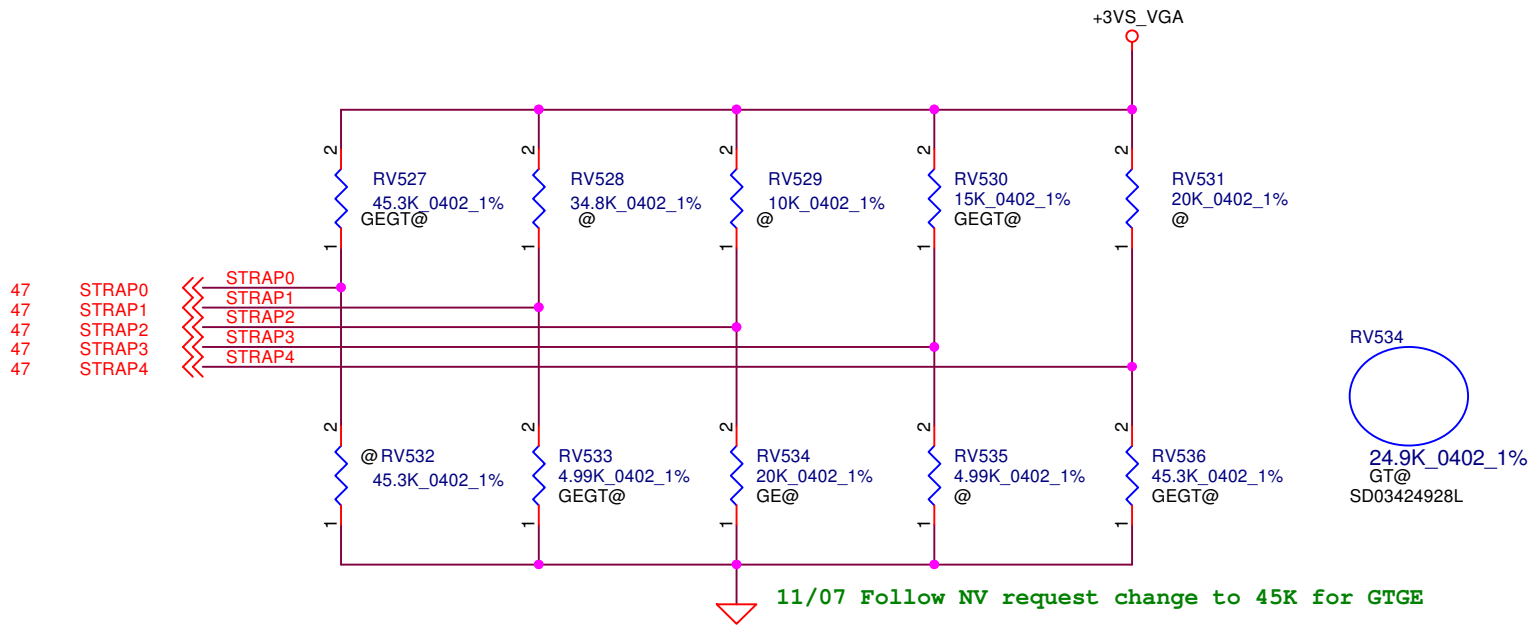
## Memory Partition C - Upper 32 bits



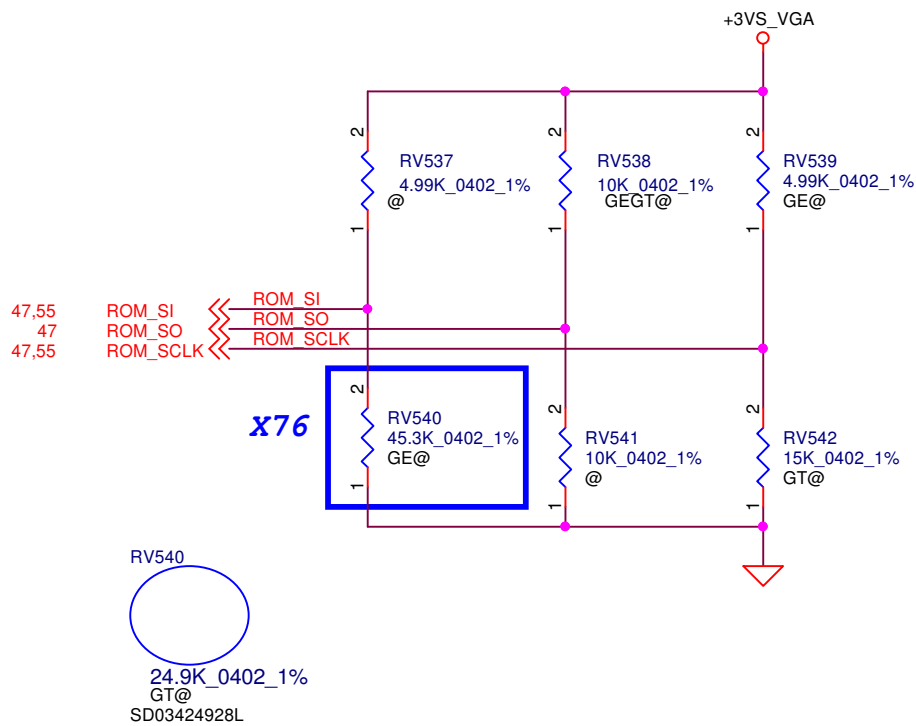
## GDDR5

### Mode H - Mirror Mode Mapping

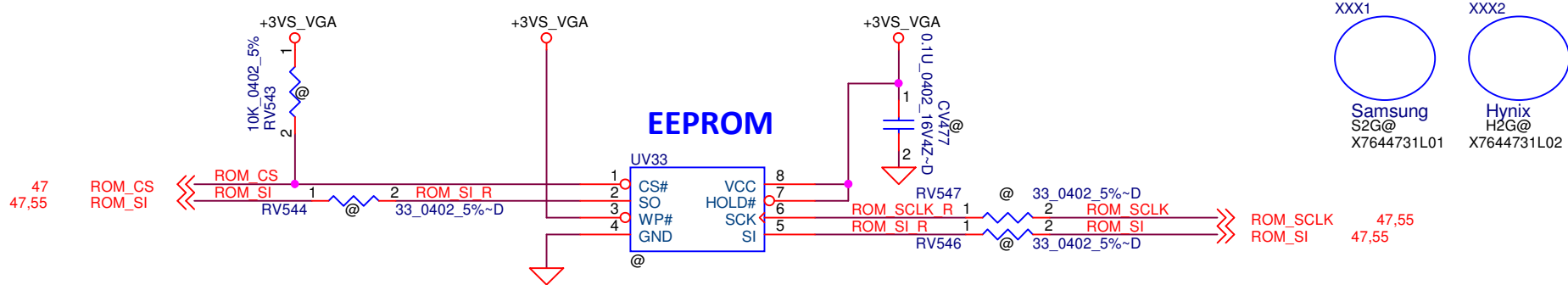
	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#



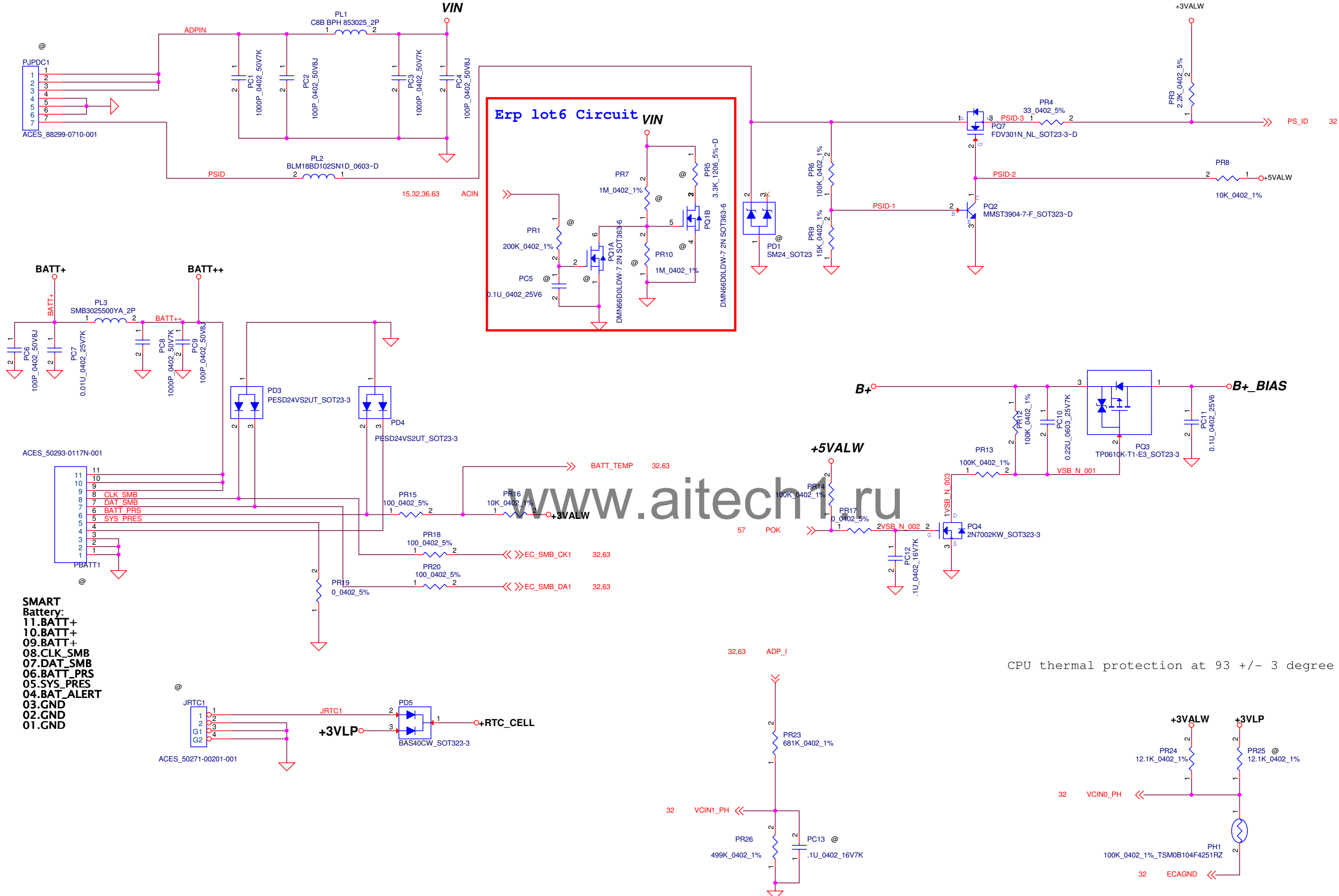
N14E-GE (ver.ES) SA00005W30L Samsung SA00005B70L  
N14P-GT (ver.ES) SA00005W20L Hynix SA00004GD1L



GPU	FB Memory gDDR5	ROM_SO	ROM_SCLK	ROM_SI	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N14P-GT	Samsung 900MHz								
	Hynix 900MHz	PU 10K	PD 15K	PD 25K	PU 45K	PD 5K	PD 25K	PU 15K	PD 45K
N14E-GE	Samsung 900MHz	PU 10K	PU 5K	PD 45K	PU 45K	PD 5K	PD 20K	PU 15K	PD 45K
	Hynix 900MHz								



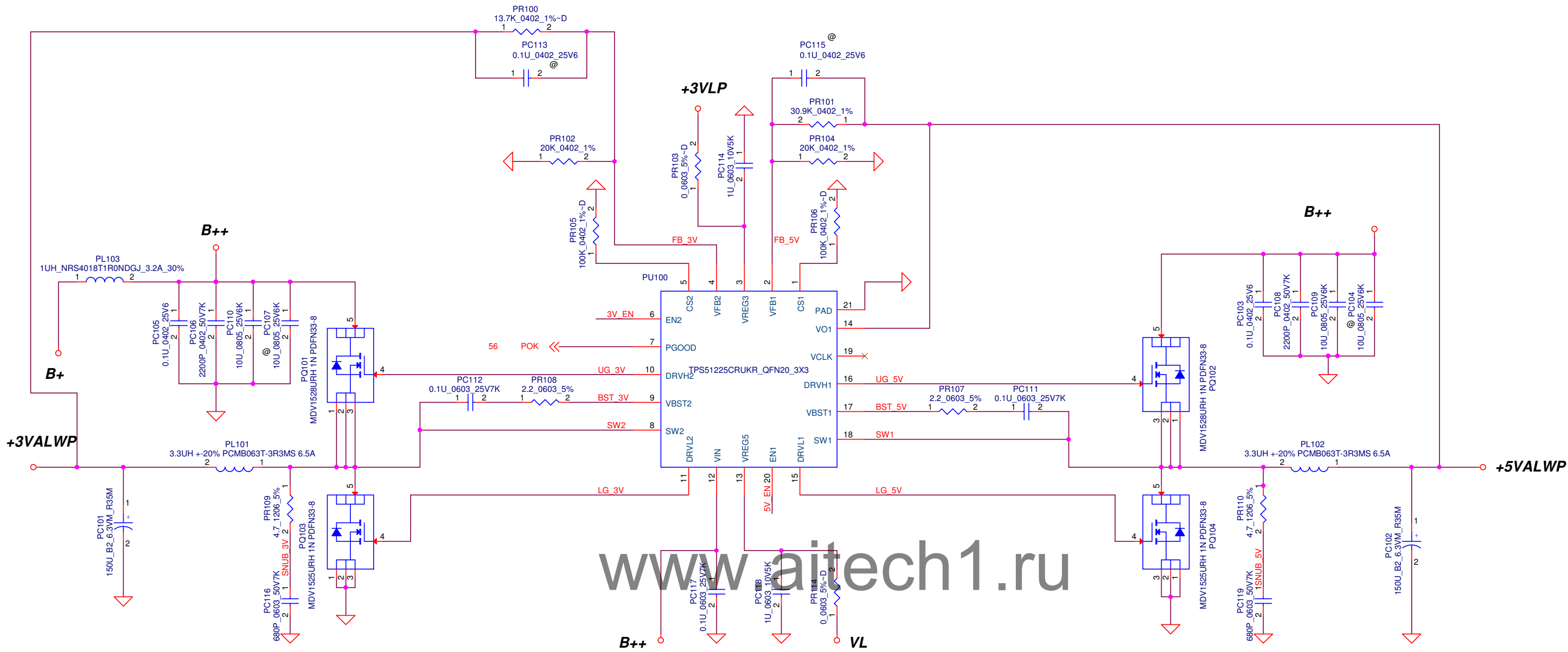
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Issued Date	2012/05/10	Deciphered Date	2013/12/31	Title		
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				Custom	LA-9201P	0.1
				Date:	Friday, August 17, 2012	Sheet 55 of 66



SMART  
Battery:  
11.BATT+  
10.BATT+  
09.BATT+  
08.CLK\_SMB  
07.DAT\_SMB  
06.BATT\_PRS  
05.SYS\_PRS  
04.BAT\_ALERT  
03.GND  
02.GND  
01.GND

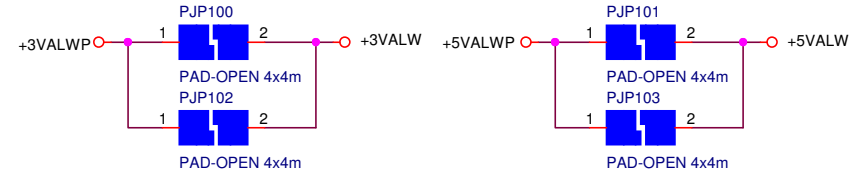
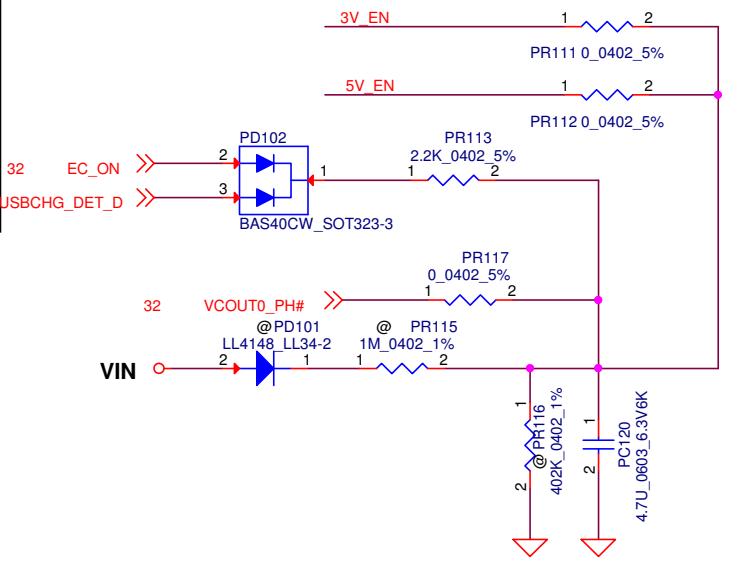
CPU thermal protection at 93 +/- 3 degree C

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/01/17	Deciphered Date	2013/01/16	Title	PWR-DCIN / BATT CONN / OTP
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				Rev	0.1
Date: Friday, August 10, 2012		Sheet 56		of 66	



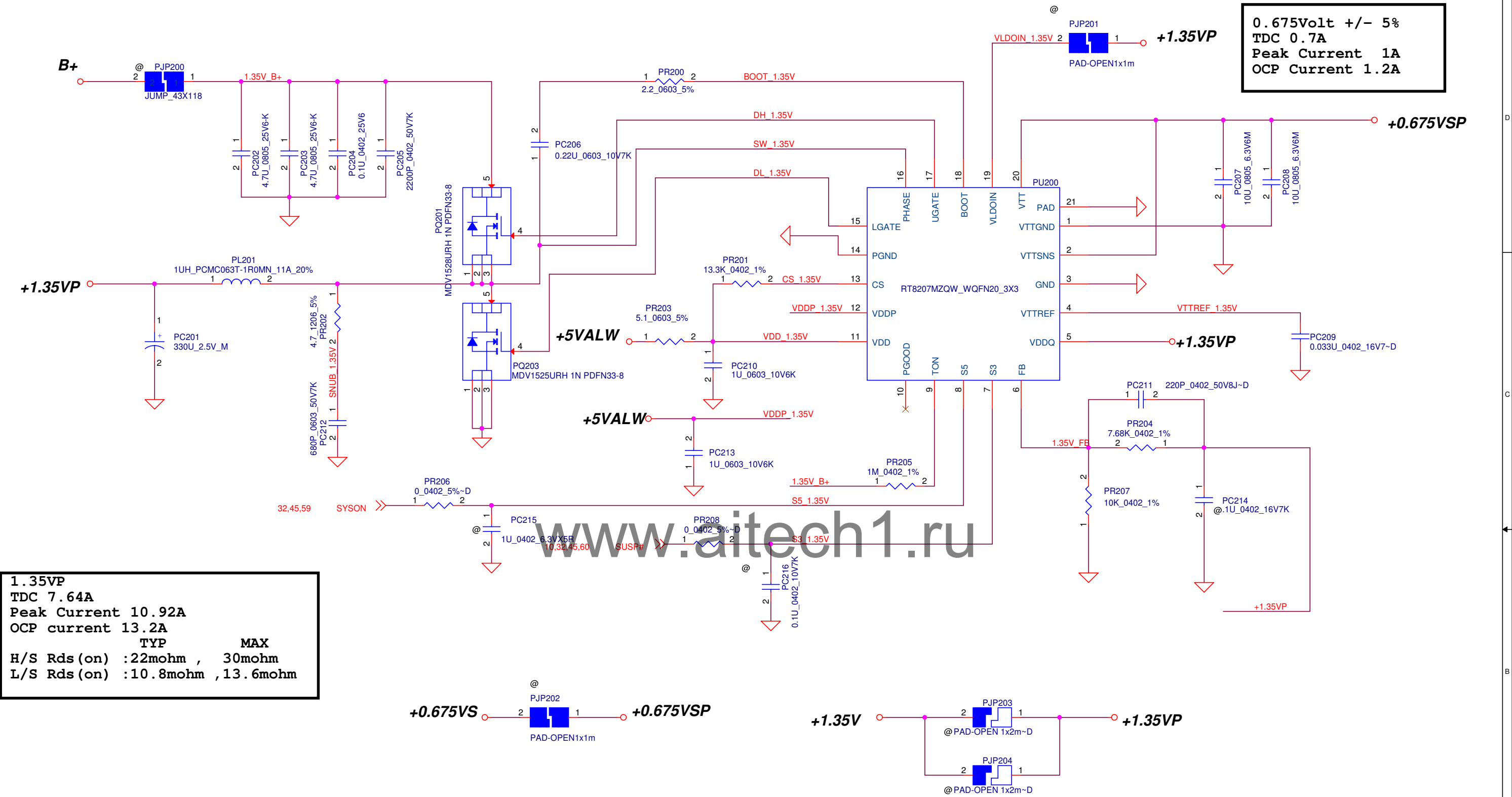
**3VALWP**  
TDC 5.95A  
Peak Current 8.5A  
OCP current 10.2A  
TYP MAX  
H/S Rds(on) : 22mohm , 30mohm  
L/S Rds(on) : 10.8mohm , 13.6mohm

**5VALWP**  
TDC 5.96A  
Peak Current 8.51A  
OCP current 10.2A  
TYP MAX  
H/S Rds(on) : 22mohm , 30mohm  
L/S Rds(on) : 10.8mohm , 13.6mohm



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				Date:	Friday, August 10, 2012
				Sheet	57 of 66
				Rev	0.1



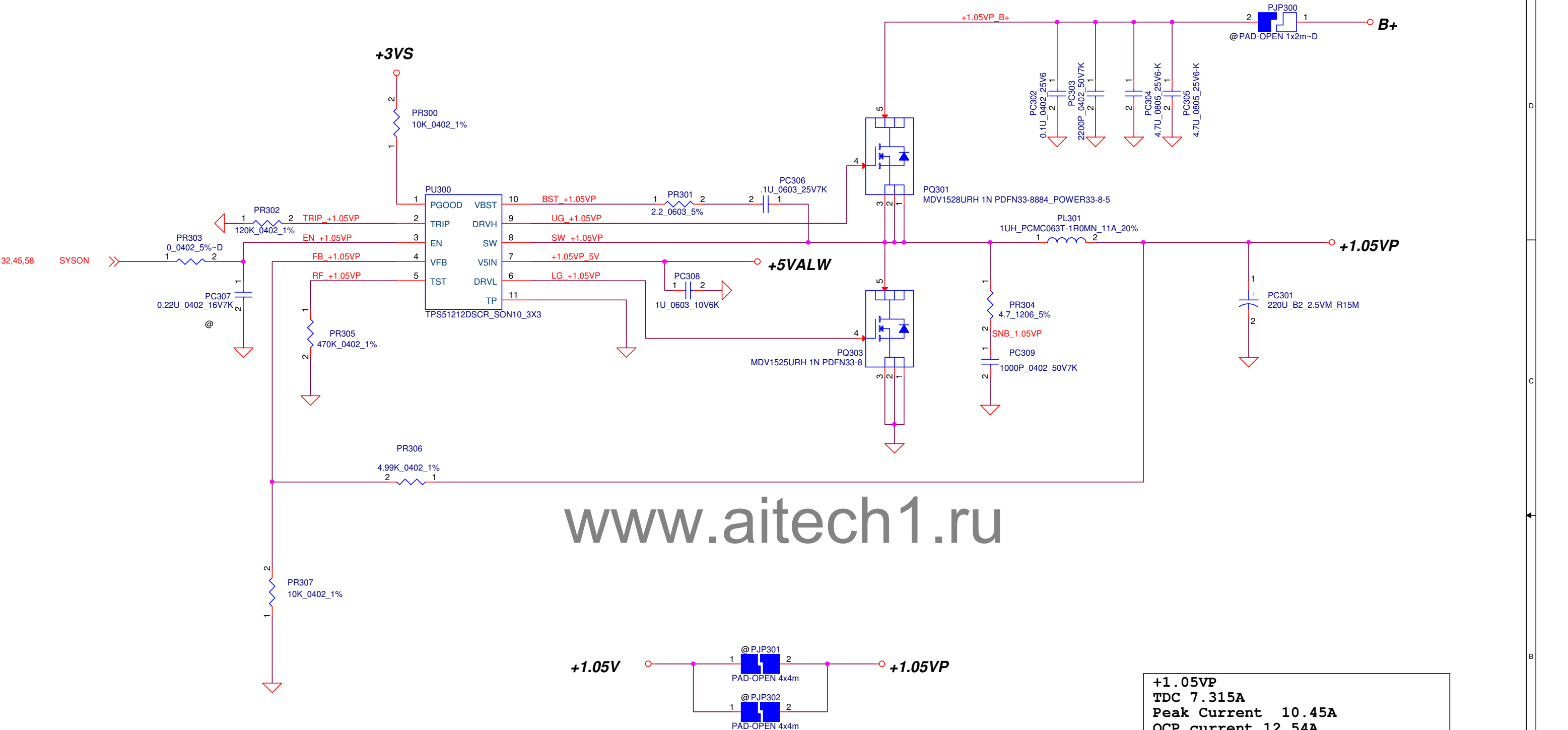


1.35VP  
TDC 7.64A  
Peak Current 10.92A  
OCP current 13.2A

	TYP	MAX
H/S Rds (on)	:22mohm	, 30mohm
L/S Rds (on)	:10.8mohm	, 13.6mohm

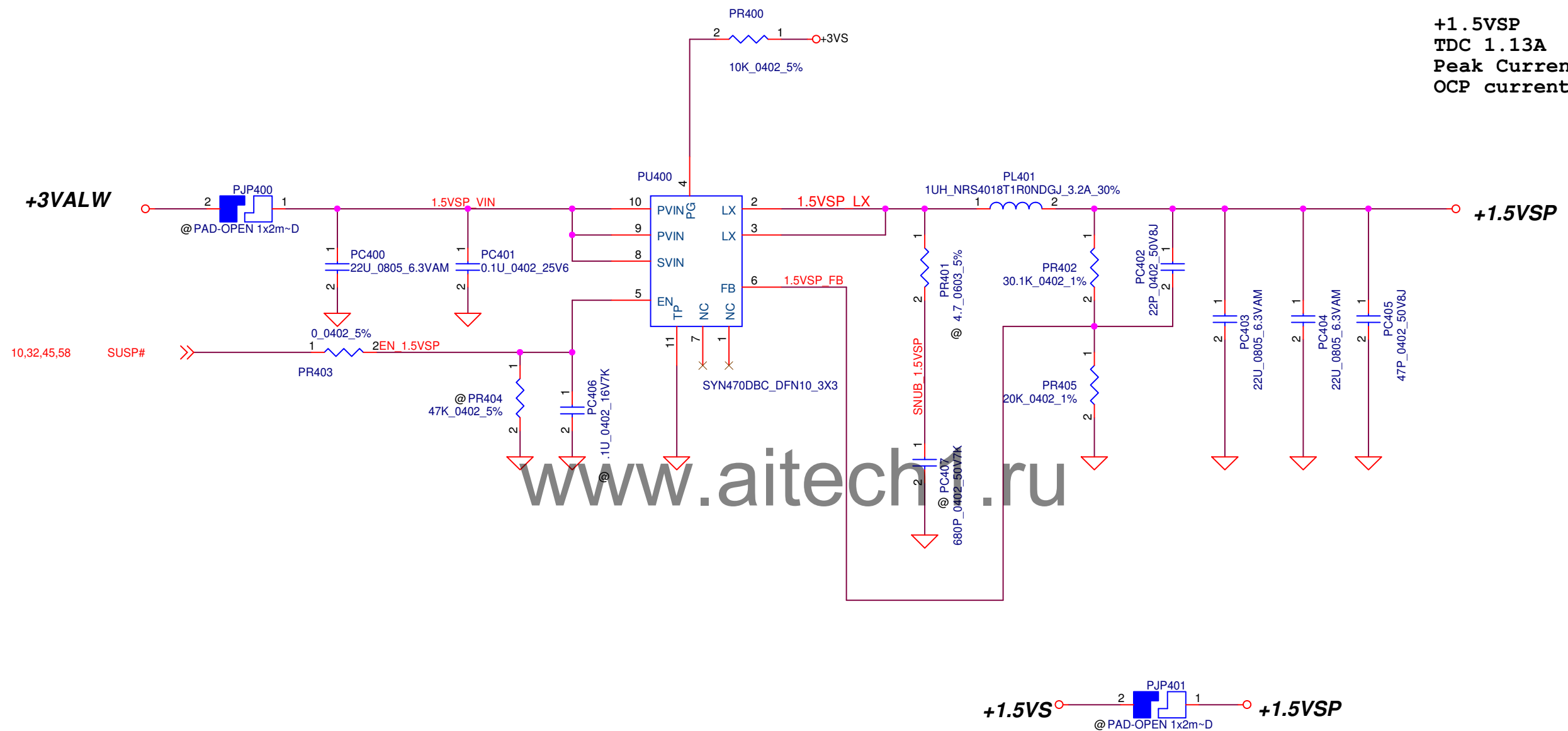
0.675Volt +/- 5%  
TDC 0.7A  
Peak Current 1A  
OCP Current 1.2A

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+1.05VP	
TDC 7.315A	
Peak Current	10.45A
OCF current	12.54A
TYP MAX	
H/S Rds (on)	: 22mohm , 30mohm
L/S Rds (on)	: 10.8mohm , 13.6mohm

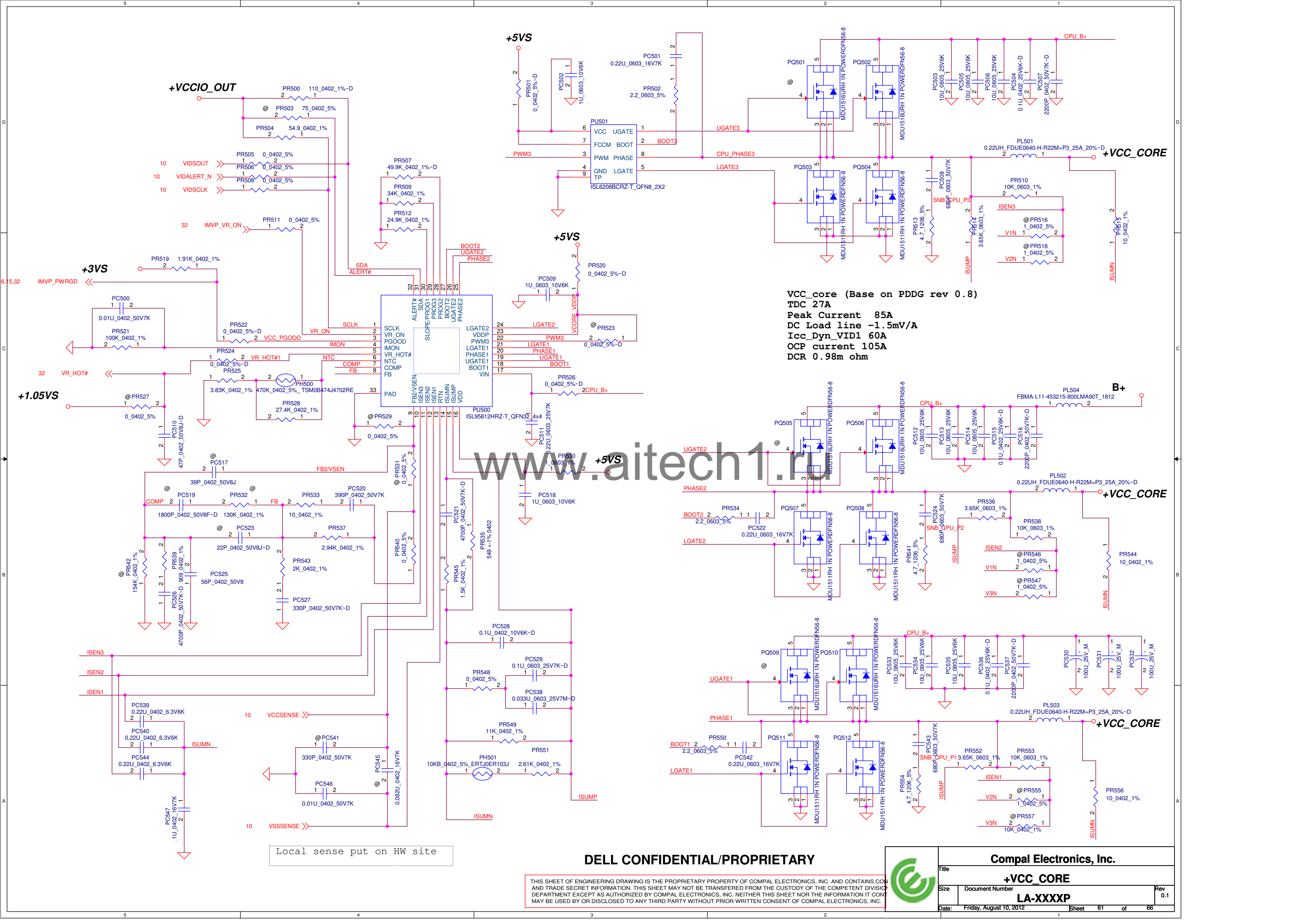
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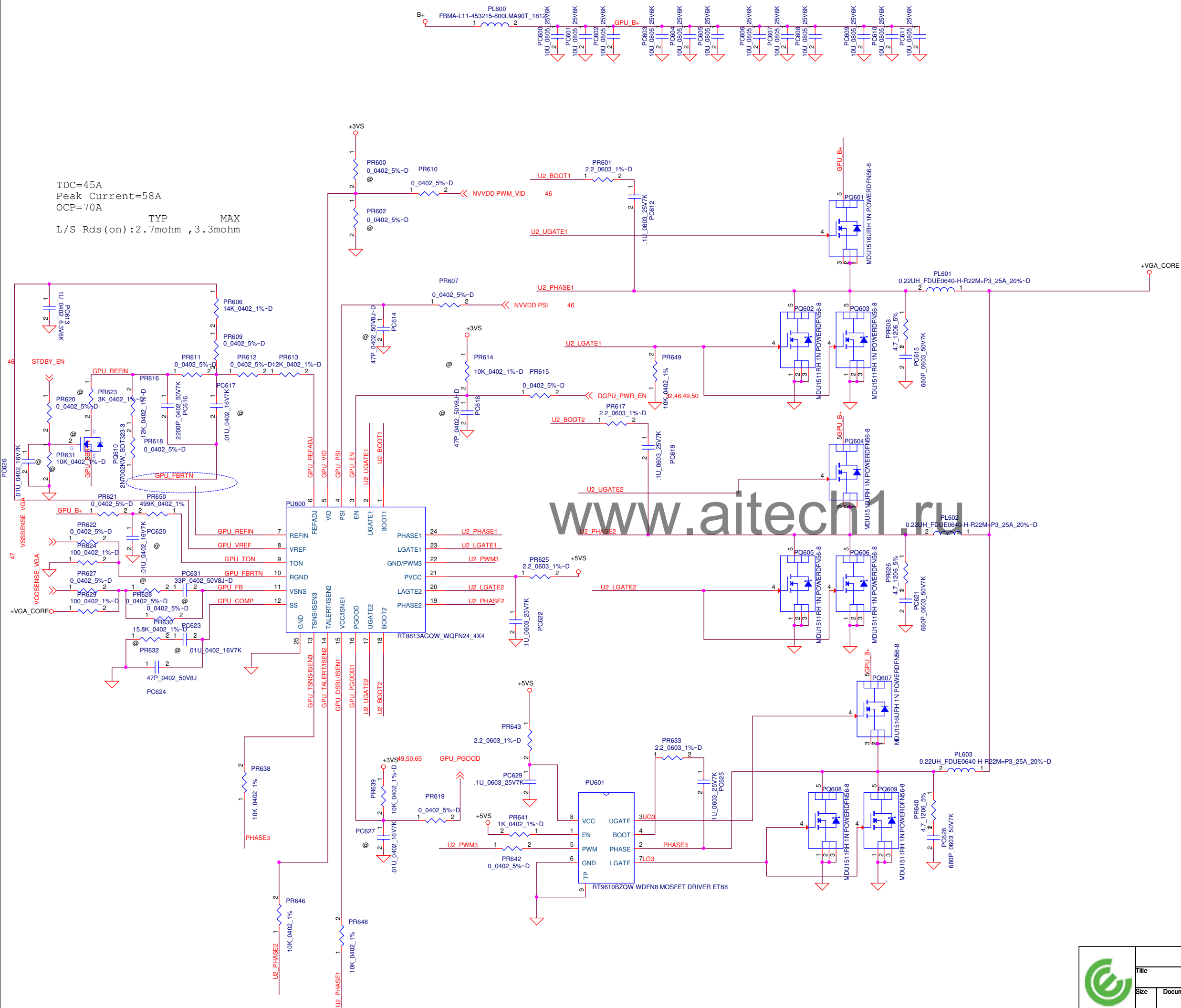
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+VCC_CORE			
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TDC=45A  
Peak Current=58A  
OCP=70A

	TYP	MAX
L/S Rds(on):	2.7mohm	3.3mohm



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Title
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+VGA\_CORE

Size

Document Number

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Date \_\_\_\_\_

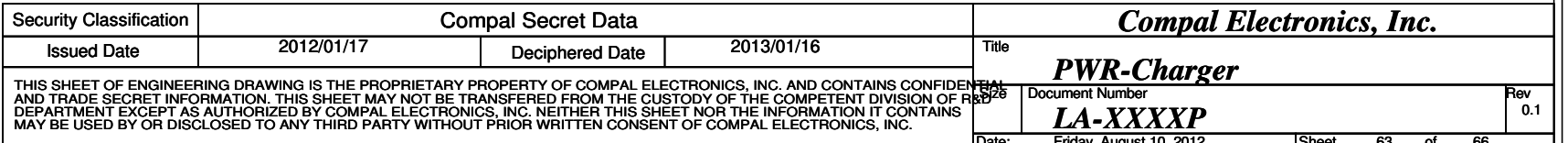
Friday, August 10, 2012

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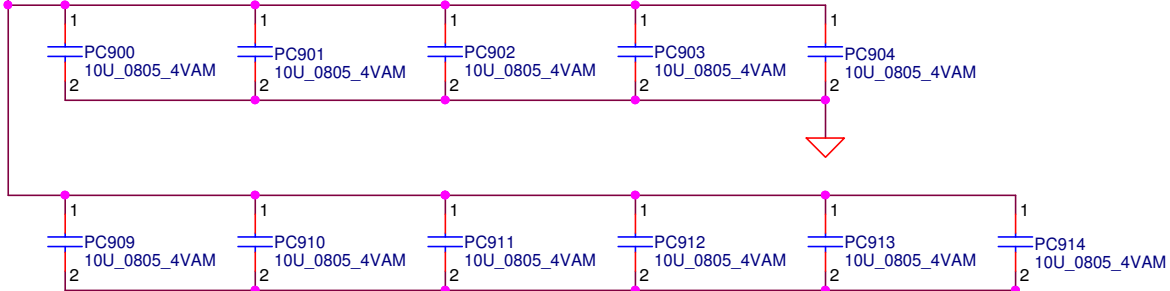
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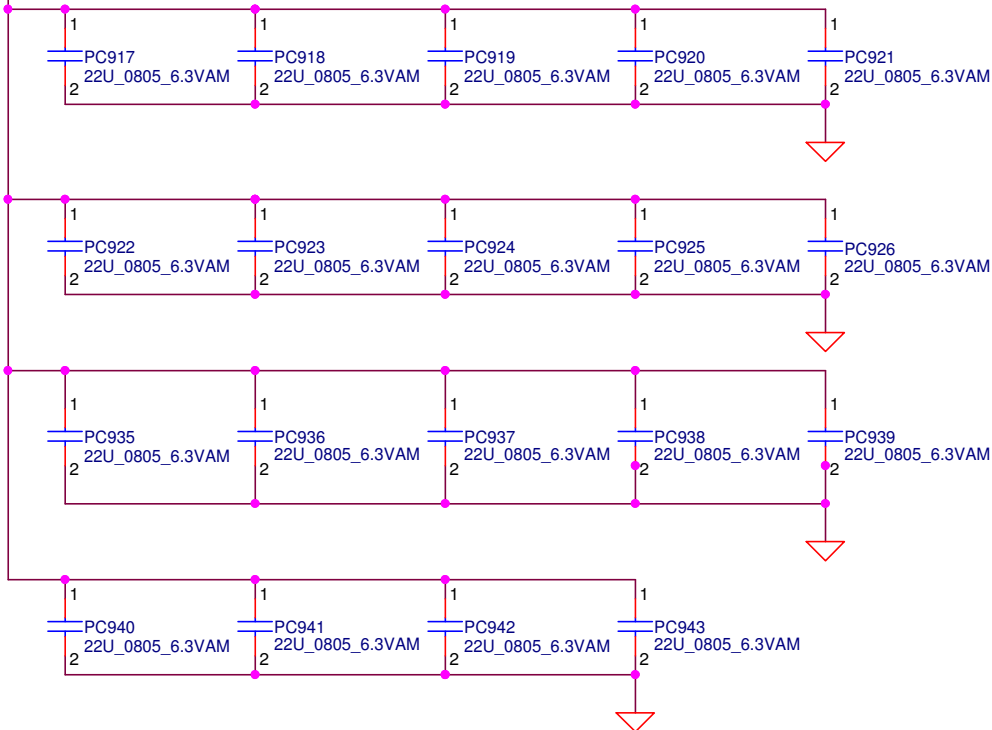


Based on PDDG rev 0.7 Table 5-1.

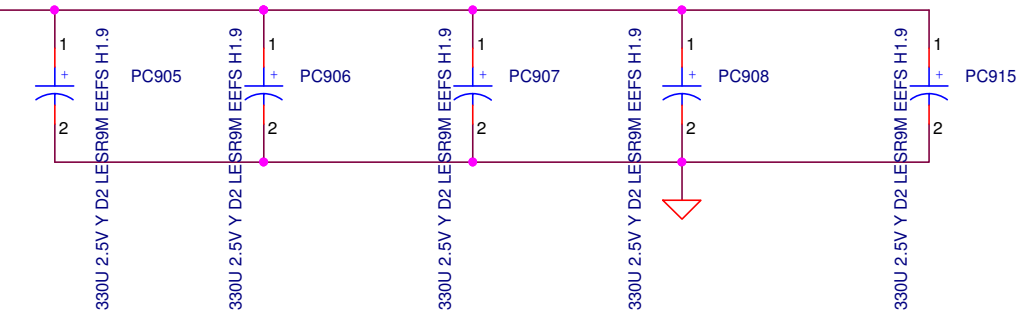
+VCC\_CORE



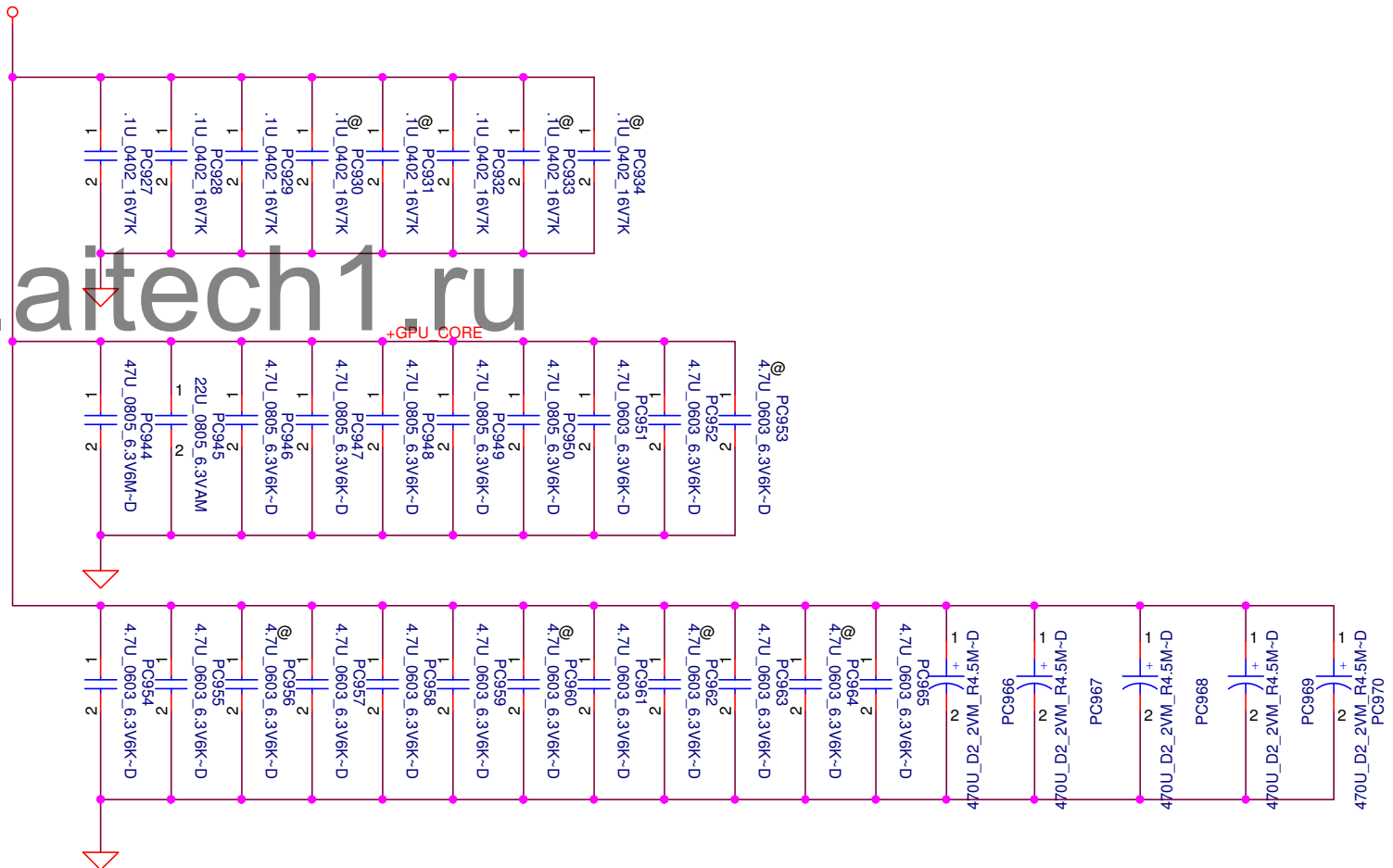
+VCC\_CORE



+VCC\_CORE



+VGA\_CORE



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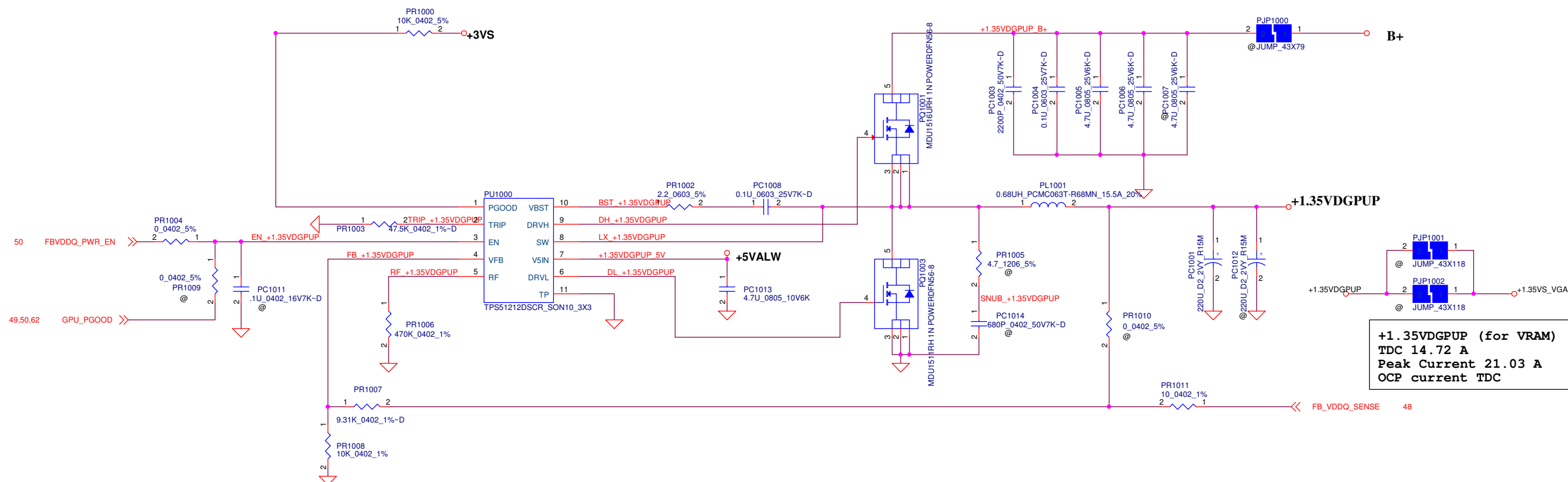
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	56	Power	7/24	Compal	HW and Power has the same part	PD5 pin1 change from +RTC_BATT to +RTC_CELL	
2	57	Power	7/24	Compal	Shortage issue	PC111、PC112 change from SE042104M80 to SE042104K8L	
3	56 63	Power	7/24	Compal	Shortage issue	PQ1,PQ710,PQ716,PQ717,PQ718 change from SB000000600 to SB000000DH0L	
4	56	Power	7/24	Compal	Adapter protect function	PR23 change from 340K ohm to 681K ohm	
5	56	Power	7/24	Compal	For De-rating	PR530 change size from 0402 to 0603	
6	57	Power	7/30	Compal	For OTP	Del PD100.Add PR117	
7	64	Power	7/30	Compal	Update Memo	Change SGA0000420L to SGA0000268L PC905,PC906,PC907,PC908,PC915	
8	62	Power	7/30	Compal	For VGA CORE	Change PU600 from UP1642 to RT8831A Change PU601 from UP1909 to RT9610B	
9	62	Power	8/1	Compal	For VGA CORE	Change PR638,PR646,PR648 from 2k to 10k Unpop PR632,PC623 Add PC624 47pF  Unpop PR628,PC631 Add PR630,PR620 o ohm  Change PR650 from 68.1k to 499k Change PC616 from 0.01uF to 2.2nF Add PR649 10k ohm	
10	58	Power	8/3	Compal	For 1.35V output voltage and Dfx request	Change PR204 from 8.06k to 7.65k Change PJP203,PJP204 size from 4x4m to 1x2m	
11							
14							
15							

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